Amtron Technology, Inc.

Industrial Grade 2.5” PATA SSD

AC Series

Product Datasheet

V1.2

Table of Contents

1. Introduction 4
1.1. Description 4
1.2. Product Features 4
1.3. Product Dimension 5
1.4. Block Diagram 6
2. Product Specifications 7
2.1. Specifications 7
2.2. Compliance 11
2.3. MTBF 11
3. Environmental Specifications 12
3.1. Environmental Conditions 12
3.1.1. Temperature and Humidity 12
3.1.2. Shock 13
3.1.3. Vibration 13
3.1.4. Drop 13
3.1.5. Electrostatic Discharge (ESD) 13
3.2. Certification & Compliance 14
4. Electrical Specifications 15
4.1. Supply Voltage 15
4.2. Power Consumption 15
4.3. Absolute Maximum Rating 16
4.4. DC Characteristics of 5.0V I/O Cells (Host Interface) 17
4.5. AC Characteristics 17
4.5.1. PCMCIA Interface 17
4.5.2. IDE Interface Timing (PIO Mode) 26
4.5.3. Multi Word DMA 28
4.5.4. Ultra DMA 30
5. Interface 34
5.1. Pin Assignment and Descriptions 34
5.2. Jumper Setting 37
6. Supported Commands 38
6.1. Identify Drive Information 38

6.2. CIS Information 40

7. ACRONYMS 45

8. Part Number Decoder 46

1. INTRODUCTION

1.1. Description

Amtron industrial grade AC series 2.5” PATA SSD delivers all the advantages of flash disk technology with parallel ATA (aka IDE) interface. These PATA SSDs are designed with the highest endurance Single Level Cell (SLC) NAND flash memory. PATA SSDs built with economical yet durable and reliable Multi Level Cell (MLC) NAND flash are also available. These PATA SSDs are offered in wide temperature grade (-40°C to +85°C) and standard temperature grade (0°C to +70°C). Memory capacities are available from 256MB to 64GB (SLC) , 4GB to 128GB (pSLC), and 8GB to 256GB (MLC).

1.2. Product Features

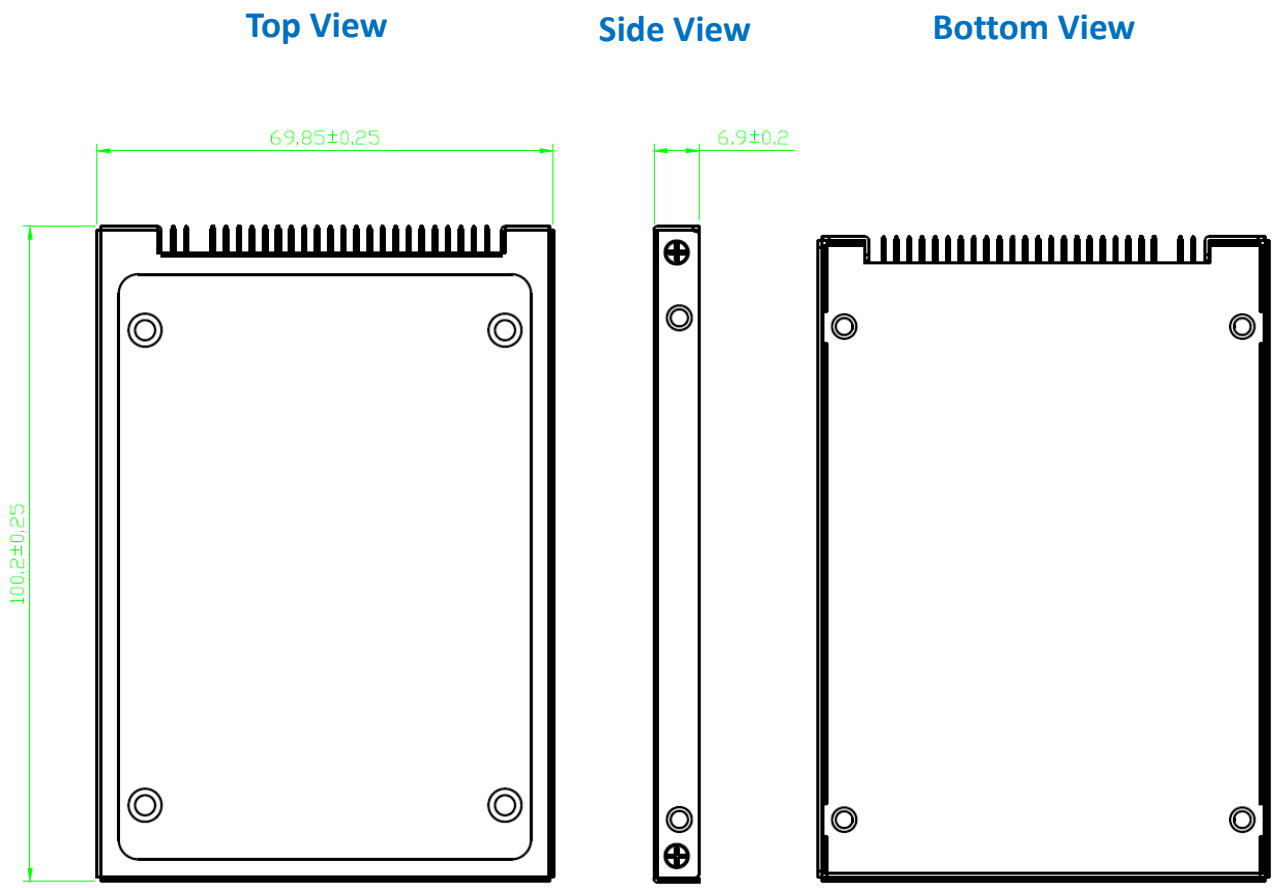
- **Flash Type**
  - SLC, MLC
- **Capacity**
  - SLC: 256MB up to 64GB
  - MLC: 8GB up to 256GB
  - pSLC: 4GB up to 128GB
- **Standard ATA/IDE Bus Interface**
  - 512 Bytes/ Sector
  - ATA command set compatible
- **Performance**
  - Read: up to 110 MB/s
  - Write: up to 80 MB/s
- **Power Consumption** [2]
  - Read mode: < 220 mA
  - Write mode: < 220 mA
  - Idle mode: < 80 mA
- **MTBF** [1]
  - SLC: 3,000,000 hours
  - MLC: 2,000,000 hours
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
- **Low Power Management**
  - Power Sleep Mode
- **Temperature Range**
  - Operation (Standard): 0°C ~ 70°C
  - Operation (Wide): -40°C ~ 85°C
  - Storage: -40°C ~ 85°C
- **Compliant**
  - RoHS
  - CE & FCC

Notes:

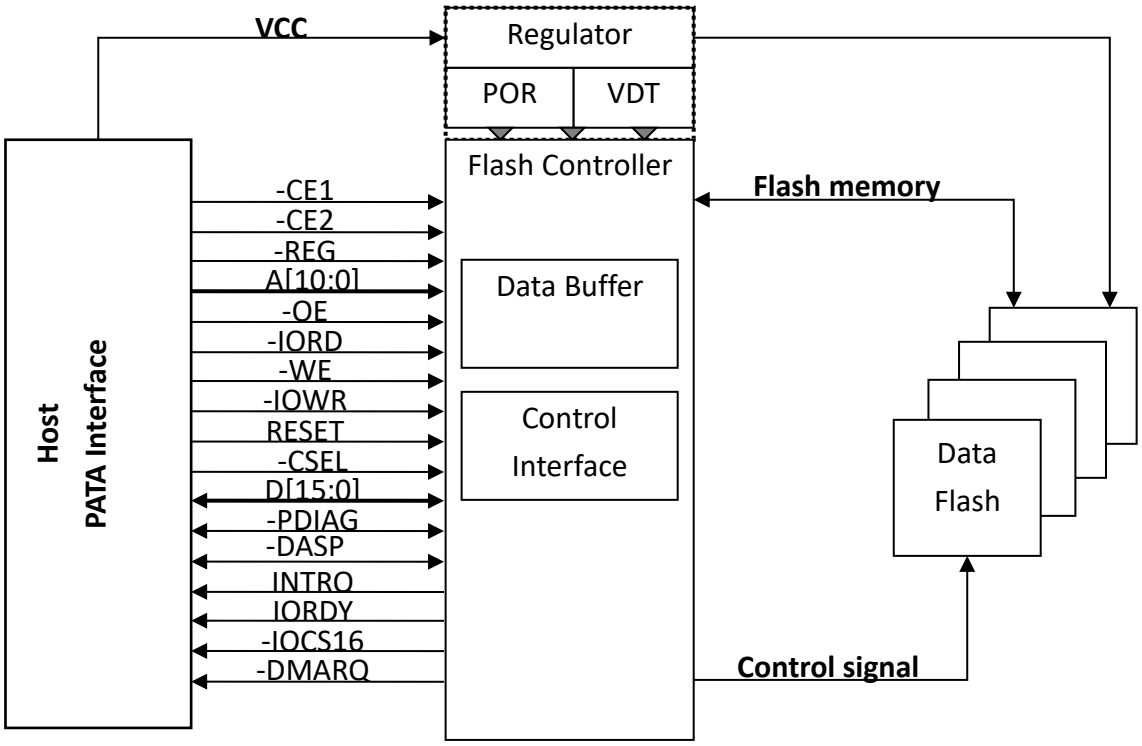
1. A lower MTBF is expected for higher capacity drives. To be conservative, the lowest MTBF is reported in this document
2. Please see Section 4.2 “Power Consumption” for details.

1.3. Product Dimension

100.20mm (L) x 69.85mm (W) x 6.90mm (H)



1.4. Block Diagram



2.5” PATA SSD Block Diagram

2. PRODUCT SPECIFICATIONS

2.1. Specifications

- **Capacity**
  - SLC: From 256MB up to 64GB
  - MLC: From 8GB up to 256GB
  - pSLC: From 4GB up to 128GB
- **Standard 2.5’’ form factor**
- **Standard ATA/IDE Bus Interface**
  - 512 Bytes/Sector
  - Compatible with ATA command set
- **Data Transfer Mode:**
  - Support data transfer up to PIO mode 4
  - Support data transfer up to Multiword DMA mode 4
  - Support data transfer up to Ultra DMA mode 6
- **NAND Flash Interface**
  - Support SLC / MLC NAND flash memory
  - Support 16KB data per page NAND flash memory
- **ECC Scheme**
  - Up to 72 bits / 1K Byte
- **Operating Voltage:** 5V
- **Support Static/Dynamic Wear Leveling function**
- **Light weight and noiseless**

- **Performance**
  - **SLC**

Capacity	Flash Structure	Flash Type	Sequential (MB/s)	
			Read	Read
256MB	256MB x 1	24nm TSOP	20	10
	128MB x 2	24nm TSOP	35	20
512MB	512MB x 1	32nm TSOP	30	20
1GB	1GB x 1	32nm TSOP	30	20
2GB	1GB x 2	32nm TSOP	60	30
4GB	4GB x 1	24nm TSOP	35	30
	2GB x 2	32nm TSOP	60	45
8GB	4GB x 2	24nm TSOP	70	60
	8GB x 1	24nm TSOP	40	35
	8GB x 1	24nm BGA	110	70
16GB	4GB x 4	24nm TSOP	80	70
	8GB x 2	24nm TSOP	80	70
	16GB x 1	24nm TSOP	40	35
	8GB x 2	24nm BGA	110	70
	16GB x 1	24nm BGA	110	70
32GB	8GB x 4	24nm TSOP	80	70
	16GB x 2	24nm TSOP	80	70
	16GB x 2	24nm BGA	110	70
	32GB x 1	24nm BGA	110	70
64GB	16GB x 4	24nm TSOP	80	70
	32GB x 2	24nm BGA	110	70

Notes:

1. The performance was measured CrystalDiskMark6.0 with test data size is 1GB
2. The performance was estimated based on Kioxia NAND flash.
3. Performance may differ according to flash configuration and platform.

- **MLC**

Capacity	Flash Structure	Flash Type	Sequential (MB/s)	
			Read	Write
8GB	8GB x 1	15nm TSOP	70	25
16GB	16GB x 1	15nm TSOP	70	25
	8GB x 2	15nm TSOP	90	40
32GB	8GB x 4	15nm TSOP	90	60
	16GB x 2	15nm TSOP	90	45
	32GB x 1	15nm BGA	90	45
64GB	16GB x 4	15nm TSOP	90	65
	32GB x 2	15nm TSOP	90	65
	32GB x 2	15nm BGA	90	75
	64GB x 1	15nm BGA	110	65
128GB	32GB x 4	15nm TSOP	100	70
	64GB x 2	15nm TSOP	100	70
	64GB x 2	15nm BGA	110	70
	128GB x 1	15nm BGA	110	70
256GB	64GB x 4	15nm TSOP	90	80
	128GB x 2	15nm BGA	110	65

Notes:

1. The performance was measured CrystalDiskMark6.0 with test data size is 1GB
2. The performance was estimated based on Kioxia NAND flash.
3. Performance may differ according to flash configuration and platform.

■ **pSLC**

Capacity	Flash Structure	Flash Type	Sequential (MB/s)	
			Read	Write
4GB	8GB x 1	15nm TSOP	70	25
8GB	16GB x 1	15nm TSOP	70	25
	8GB x 2	15nm TSOP	90	40
16GB	8GB x 4	15nm TSOP	90	60
	16GB x 2	15nm TSOP	90	45
	32GB x 1	15nm BGA	90	45
32GB	16GB x 4	15nm TSOP	90	65
	32GB x 2	15nm TSOP	90	65
	32GB x 2	15nm BGA	90	75
	64GB x 1	15nm BGA	110	65
64GB	32GB x 4	15nm TSOP	100	70
	64GB x 2	15nm TSOP	100	70
	64GB x 2	15nm BGA	110	70
	128GB x 1	15nm BGA	110	70
128GB	64GB x 4	15nm TSOP	90	80
	128GB x 2	15nm BGA	110	65

Notes:

1. The performance was measured CrystalDiskMark6.0 with test data size is 1GB
2. The performance was estimated based on Kioxia NAND flash.
3. Performance may differ according to flash configuration and platform.

2.2. Compliance

Up to ATA/ATAPI-8 (Including S.M.A.R.T)

2.3. MTBF

MTBF (mean time between failures) is a measure of how reliable a hardware product is. Its value represents the average time between a failure repair and the next failure. The unit of MTBF is typically in hours. The higher the MTBF value, the higher the reliability of the product. Please note that a lower MTBF is expected for higher capacity drives. To be conservative, the lowest MTBF is reported in this document. The predicted MTBF for Amtron 2.5” SLC PATA SSD is 3,000,000 hours.

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

- Temperature:
  - Storage: -40°C to 85°C
  - Operational (Standard grade): 0°C to 70°C
  - Operational (Wide grade): -40°C to 85°C
- Humidity:
  - Standard grade: RH 90% under 40°C (operational)
  - Wide grade: RH 95% under 55°C (operational)

■ **High Temperature Test Condition**

	Temperature	Humidity	Test Time
Operation (Standard)	70°C	0% RH	72 hours
Operation (Wide)	85°C	0% RH	72 hours
Storage (Standard)	85°C	0% RH	72 hours
Storage (Wide)	85°C	0% RH	168 hours

Result: No abnormality is detected.

■ **Low Temperature Test Condition**

	Temperature	Humidity	Test Time
Operation (Standard)	0°C	0% RH	72 hours
Operation (Wide)	-40°C	0% RH	72 hours
Storage (Standard)	-40°C	0% RH	72 hours
Storage (Wide)	-40°C	0% RH	168 hours

Result: No abnormality is detected.

■ **High Humidity Test Condition**

	Temperature	Humidity	Test Time
Operation (Standard)	40°C	93% RH	24 hours
Operation (Wide)	55°C	95% RH	72 hours
Storage (Standard)	40°C	95% RH	72 hours
Storage (Wide)	55°C	95% RH	96 hours

Result: No abnormality is detected.

■ **Temperature Cycle Test**

	Temperature	Test Time	Cycle
Operation (Standard)	0°C	30 min	10 cycles
	70°C	30 min	
Operation (Wide)	-40°C	30 min	20 cycles
	85°C	30 min	
Storage (Standard)	-40°C	30 min	10 cycles
	85°C	30 min	
Storage (Wide)	-40°C	30 min	50 cycles
	85°C	30 min	

Result: No abnormality is detected.

3.1.2. Shock

■ **Shock Specification**

	Acceleration Force	Half Sin Pulse Duration
Operational	1500G	0.5ms

Result: No abnormality is detected when power on.

3.1.3. Vibration

■ **Vibration Specification**

	Condition		Vibration Orientation
	Frequency/Displacement	Frequency/Acceleration	
Operational	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G	X, Y, Z axis/60 min for each

Result: No abnormality is detected when power on.

3.1.4. Drop

■ **Drop Specification**

	Height of Drop	Number of Drop
Non-operational	80cm free fall	6 face of each unit

Result: No abnormality is detected when power on.

3.1.5. Electrostatic Discharge (ESD)

■ **Contact ESD Specification**

Device	Temperature	Relative Humidity	+/- 4KV	Result
2.5” PATA SSD	24.0°C	49% (RH)	Device functions are affected, but EUT will be back to its normal or operational state automatically.	PASS

3.2. Certification & Compliance

- RoHS
- CE / FCC

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Parameter	Rating
Operating Voltage	5V

4.2. Power Consumption

Read	Write	Idle
220	220	80

Unit: mA

NOTES:

1. Samples were built using Kioxia NAND flash.
2. The operating voltage is 5.0V.
3. Sequential R/W is measured while testing 4000MB sequential R/W 5 times by CyrstalDiskMark.
4. Power Consumption may vary from flash configuration or platform

4.3. Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit	Remark
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+5.5	V	
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V	
3	Ta	Operating Temperature	0	+70	°C	Commercial Grade
4	Tst	Storage Temperature	-25	+85	°C	Commercial Grade
5	Ta	Operating Temperature	-40	+85	°C	Industrial Grade
6	Tst	Storage Temperature	-40	+85	°C	Industrial Grade

Parameter	Symbol	Min	TYP	MAX	Unit
V_{DD} Voltage	V_{DD}	4.5	5.0	5.5	V

4.4. DC Characteristics of 5.0V I/O Cells (Host Interface)

Table 4-1 DC Characteristics of 5.0V I/O Cells (Host Interface)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Vol	Output Low voltage	|Iol| = 4 ~ 32 mA	-	-	0.4	V
Voh	Output High voltage	|Ioh| =4 ~ 32 mA	2.4	-	-	V
Rpu	Input Pull-Up Resistance	PU=high, PD=low	200	300	450	KΩ
Rpd	Input Pull-Down Resistance	PU=high, PD=low	200	300	450	KΩ
Iin	Input Leakage Current	Vin = VCC3I or 0	-10	±1	10	µA
Ioz	Tri-state Output Leakage Current		-10	±1	10	µA

4.5. AC Characteristics

4.5.1. PCMCIA Interface

Attribute Memory Read Timing

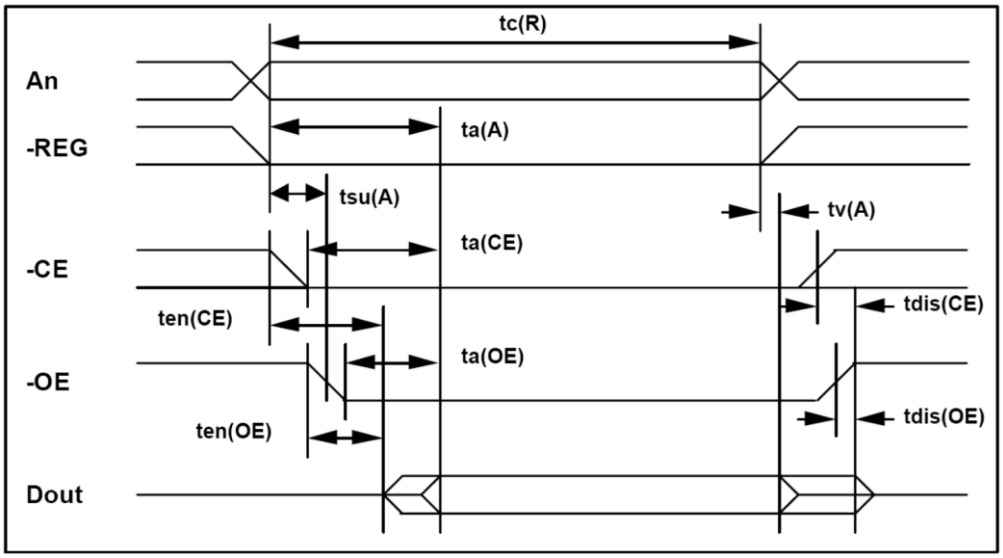


Figure 4-1 Attribute Memory Read Timing

Table 4-2 Attribute Memory Read Timing

Speed Version	Symbol	IEEE Symbol	300 ns.	
Item			Min ns.	Max ns.
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(a)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

Attribute Memory Write Timing

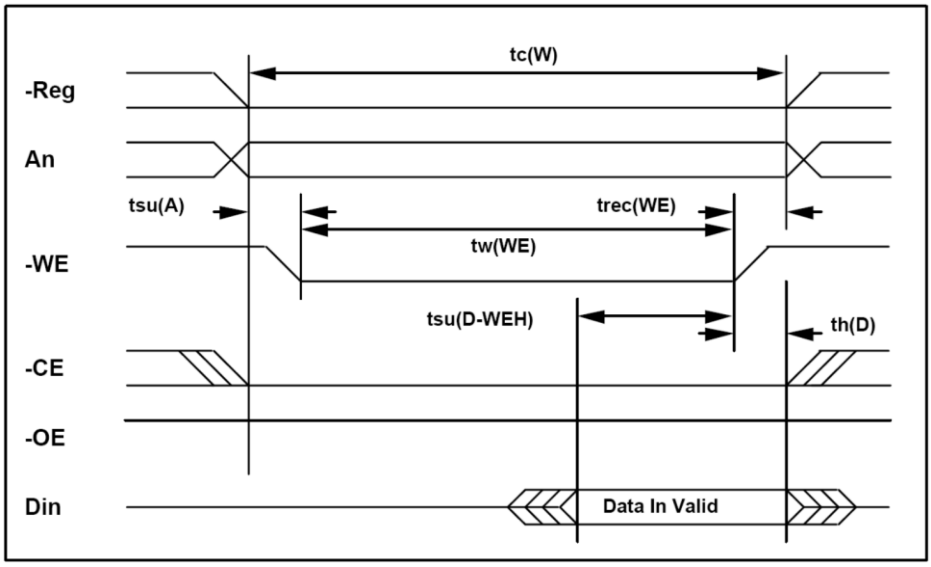


Figure 4-2 Attribute Memory Write Timing

Table 4-3 Attribute Memory Writing Timing

Speed Version	Symbol	IEEE Symbol	250 ns	
Item			Min ns	Max ns
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

Common Memory Read Timing

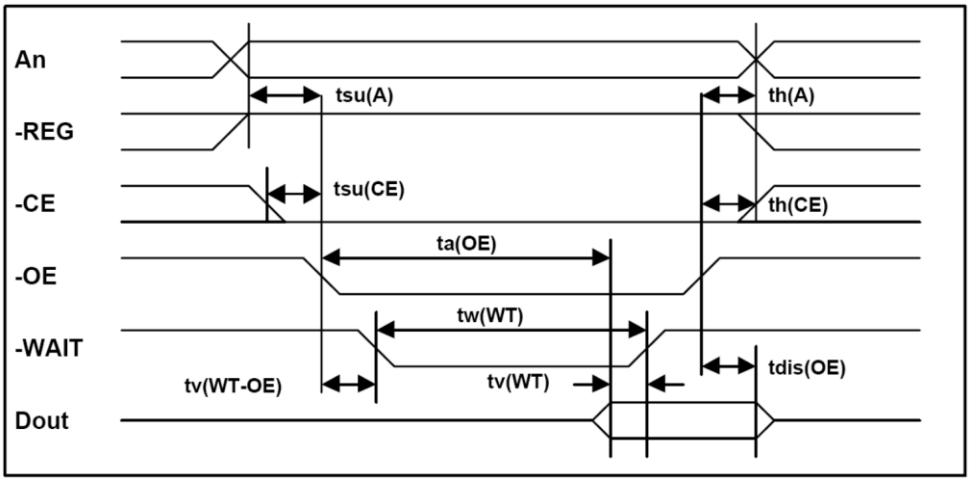


Figure 4-3 Common Memory Read Timing

Table 4-4 Common Memory Read Timing

Cycle Time Mode			250 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	

CE Hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35		35		35		na[1]
Data Setup for Wait Release	tv(WT)	tQVWTH		0		0		0		na[1]
Wait Width Time[2]	tw(WT)	tWTLWTH		350(3000 for CF+)		350(3000 for CF+)		350(3000 for CF+)		na[1]

NOTES:

1. -WAIT is not supported in this mode.
2. The maximum load on –WAIT is 1 LSTTL with 50pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The –WAIT signal may be ignored if the –OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12us but is intentionally less in this specification.

Common Memory Write Timing

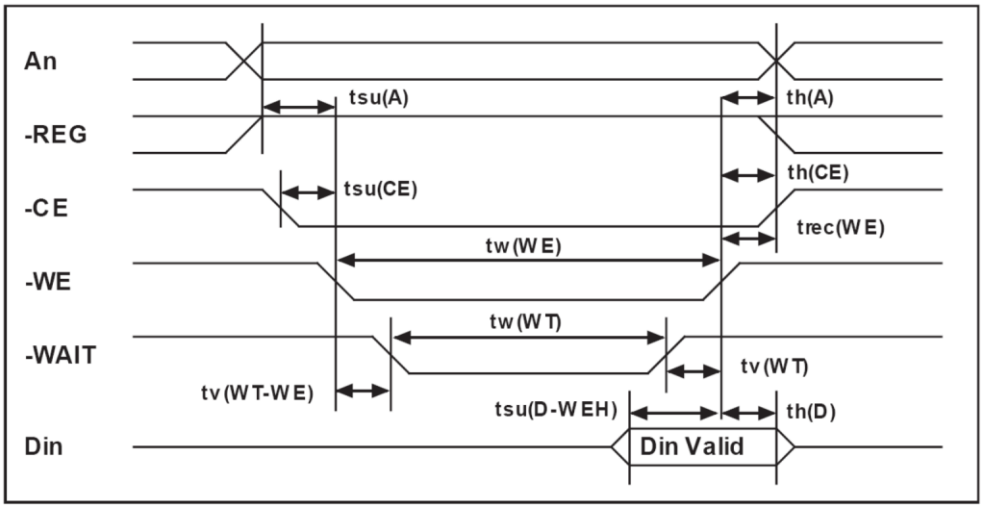


Figure 4-4 Common Memory Write Timing

Table 4-5 Common Memory Write Timing

Cycle Time Mode			250 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before WE	tsu(D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	

Cycle Time Mode			250 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		15	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV		35		35				na[1]
WE High from Wait Release	tv(WT)	tWTHWH	0		0		0		na[1]	
Wait Width Time[2]	tw(WT)	tWTLWTH		350(3000 for CF+)		350(3000 for CF+)		350(3000 for CF+)		na[1]

NOTES:

1. –WAIT is not supported in this mode.

2. The maximum load on –WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The –WAIT signal may be ignored if the –WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12us but is intentionally less in this specification.

I/O Read Timing

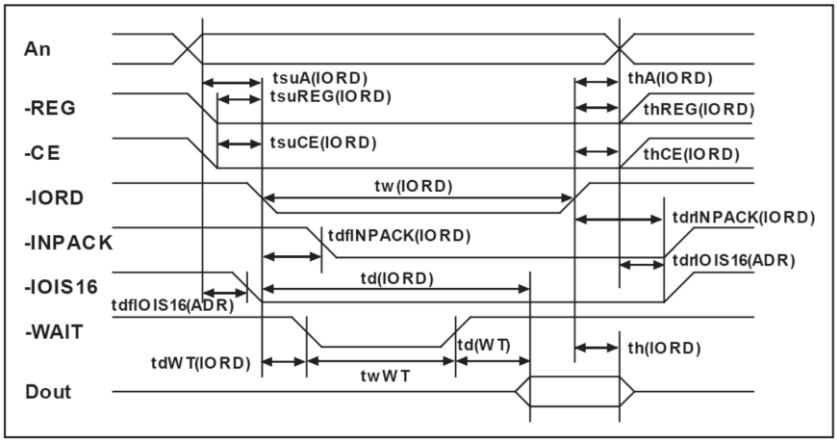


Figure 4-5 I/O Read Timing

Table 4-6 I/O Read Timing

Cycle Time Mode			250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min (ns.)**	**Max (ns.)**	**Min (ns.)**	**Max (ns.)**	**Min (ns.)**	**Max (ns.)**	**Min (ns.)**	**Max (ns.)**
Data Delay after IORD	td(IORD)	tlGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tlGHQX	0		5		5		5	
IORD W idth Time	tw(IORD)	tlGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tlGHAX	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tlGHEH	20		10		10		10	
REG Setup before IORD	tsuREG (IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG (IORD)	tlGHRGH	0		0		0		0	

INPACK Delay Falling from IORD[3]	tdfINPACK (IORD)	tlGLIAL	0	45	0	na[1]	0	na[1]	0	na[1]
INPACK Delay Rising from IORD[3]	tdrINPACK (IORD)	tlGHIAH		45		na[1]		na[1]		na[1]
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IORD[3]	tdW T(IORD)	tlGLW TL		35		35		35		na[2]
Data Delay from Wait Rising[3]	td(W T)	tW THQV		0		0		0		na[2]
Wait Width Time[3]	tw(W T)	tW TLW TH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[2]

NOTES:

1. -IOIS16 and -INPACK are not supported in this mode.
2. -WAIT is not supported in this mode.
3. Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA PC Card specification of 12µs but is intentionally less in this spec.

I/O Write Timing

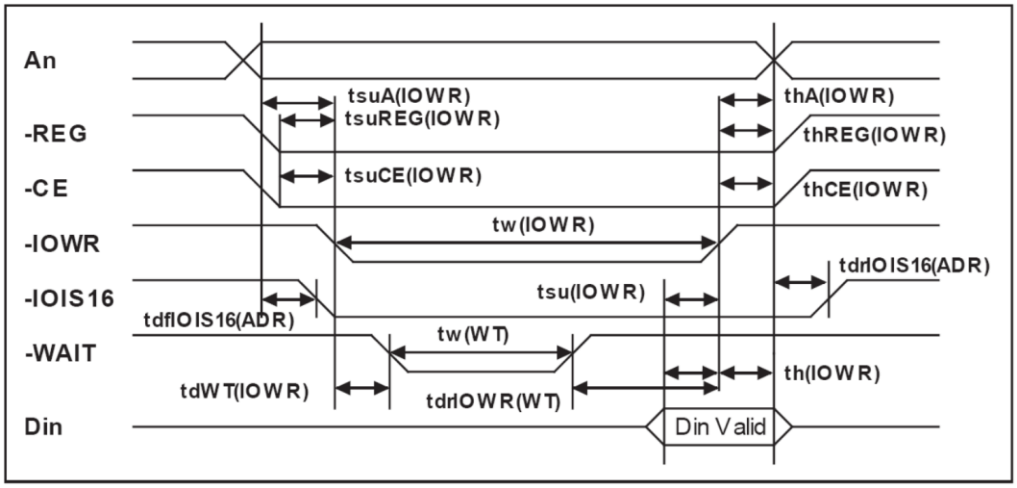


Figure 4-6 I/O Write Timing

Table 4-7 I/O Write Timing

Cycle Time Mode			255 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min (ns.)**	**Max (ns.)**	**Min (ns.)**	**Max (ns.)**	**Min (ns.)**	**Max (ns.)**	**Min (ns.)**	**Max (ns.)**
Data Setup before IOWR	tsu(IOW R)	tDVIW H	60		20		20		15	
Data Hold following IOWR	th(IOW R)	tIWHDX	30		10		5		5	
IOW R Width Time	tw(IOW R)	tIWLIW H	165		70		65		55	
Address Setup before IOW R	tsuA(IOW R)	tAVIW L	70		25		25		15	
Address Hold following IOW R	thA(IOW R)	tIWHAX	20		20		10		10	
CE Setup before IOWR	tsuCE (IOW R)	tELIW L	5		5		5		5	
CE Hold following IOWR	thCE (IOW R)	tIWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG (IOW R)	tRGLIW L	5		5		5		5	

Cycle Time Mode			255 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min (ns.)	Max (ns.)	Min (ns.)	Max (ns.)	Min (ns.)	Max (ns.)	Min (ns.)	Max (ns.)
REG Hold following IOWR	thREG (IOW R)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IOW R[3]	tdW T (IOWR)	tIWLW TL		35		35		35		na[2]
IOW R high from Wait High[3]	tdrIOW R (W T)	tW TJIWH	0		0		0		na[2]	
Wait Width Time[3]	Tw (W T)	tW TLW TH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[2]

NOTES:

1. -IOIS16 and -INPACK are not supported in this mode.
2. -WAIT is not supported in this mode.
3. The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0nsec, but minimum -IOW R width shall still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA PC Card specification of 12 µs but is intentionally less in this specification.

4.5.2. IDE Interface Timing (PIO Mode)

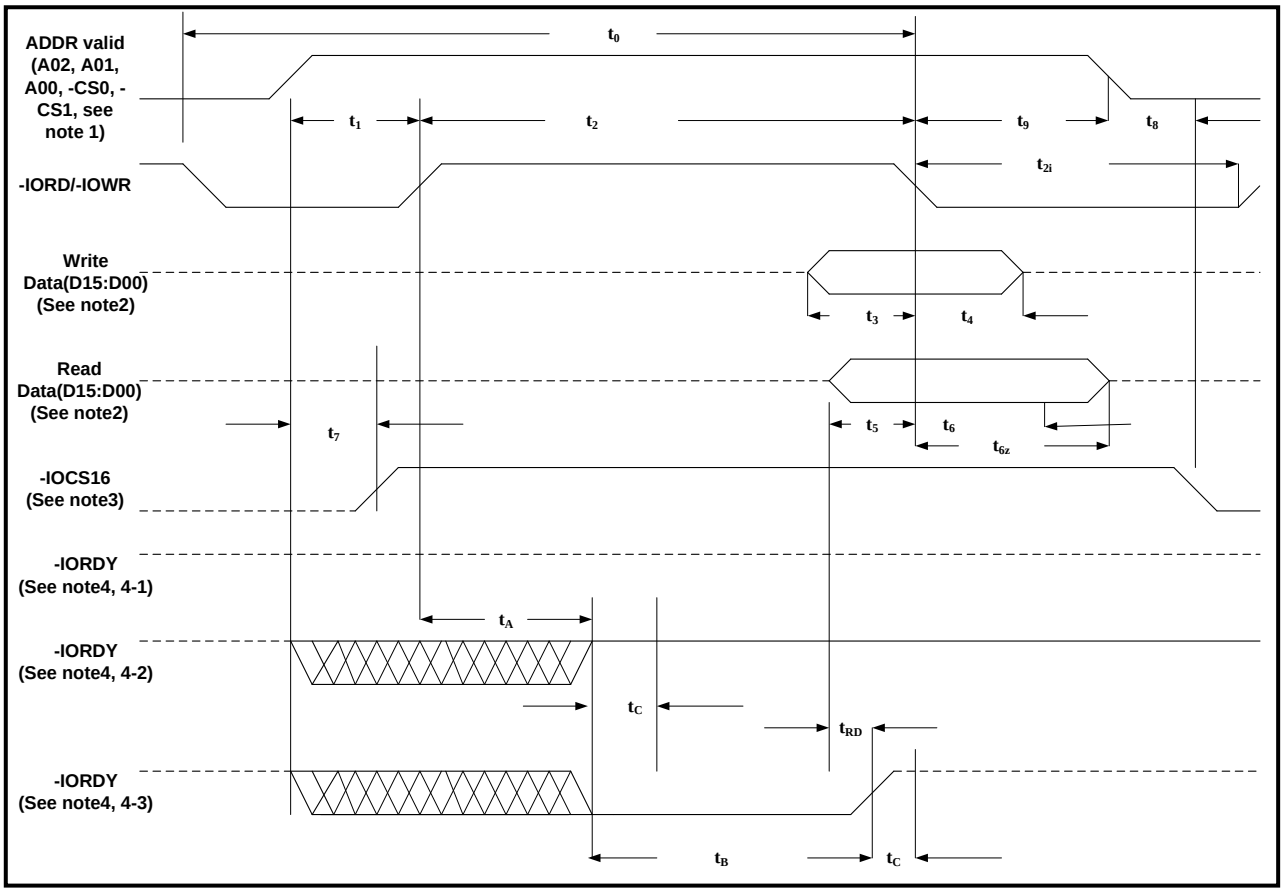


Figure 4-7 IDE Interface Timing (PIO Mode)

NOTES:

1. Device address consists of -CS0, -CS1, and A[02:00]
2. Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
3. -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
4. The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
   - Device never negates IORDY: No wait is generated.
   - Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
   - Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

Table 4-8 IDE Interface Timing

Name	Item	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Note
t0	Cycle time (min)	600	383	240	180	120	100	80	1
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	1
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55	1
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	25	20	1
t3	-IOWR data setup (min)	60	45	30	30	20	20	15	
t4	-IOWR data ho ld (min)	30	20	15	10	10	5	5	
t5	-IORD data setup (min)	50	35	20	20	20	15	10	
t6	-IORD data hold (min)	5	5	5	5	5	5	5	
T6Z	-IORD data tristate (max)	30	30	30	30	30	20	20	2
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	4
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	4
t9	-IORD/-IOWR to address valid ho ld	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially lo w after tA	0	0	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	na5	na5	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na5	na5	
tC	IORDY assertion to release (max)	5	5	5	5	5	na5	na5	

NOTES:

All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0nsec, but minimum -IORD width shall still be met.

1. t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device’s identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

2. This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).
3. The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the CompactFlash Storage Card is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.
4. t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.
5. IORDY is not supported in this mode.

4.5.3. Multi Word DMA

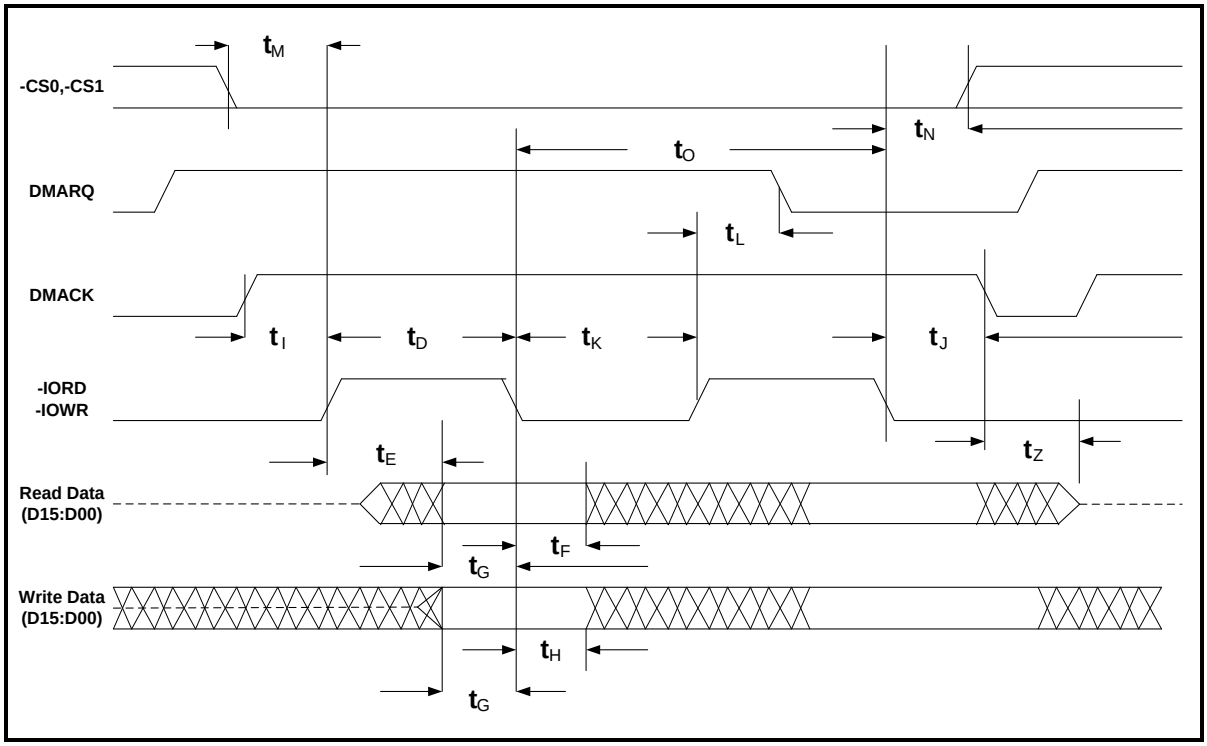


Figure 4-8 Multi Word DMA

NOTES:

All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

1. If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.
2. This signal may be negated by the host to suspend the DMA transfer in progress.

Table 4-9 MDMA Mode Timing Table

Item		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note
	Symbol	(ns)	(ns)	(ns)	(ns)	(ns)	
t_0	Cycle time (min)	480	150	120	100	80	1
t_D	-IORD / -IOWR asserted width (min)	215	80	70	65	55	1
t_E	-IORD data access (max)	150	60	50	50	45	
t_F	-IORD data hold (min)	5	5	5	5	5	
t_G	-IORD / -IOWR data setup (min)	100	30	20	15	10	
t_H	-IOWR data hold (min)	20	15	10	5	5	
t_I	DMACK to -IORD/-IOWR setup (min)	0	0	0	0	0	
t_J	-IORD / -IOWR to -DMACK hold (min)	20	5	5	5	5	
t_{KR}	-IORD negated width (min)	50	50	25	25	20	1
t_{KW}	-IOWR negated width (min)	215	50	25	25	20	1
t_{LR}	-IOWR to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	35	35	
t_M	CS(1:0) valid to -IORD/-IOWR	50	30	25	10	5	
t_N	CS(1:0) hold	15	10	10	10	10	
t_Z	-DMACK	20	25	25	25	25	

NOTE:

1. t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_{KR} and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D, t_{KR} and t_{KW} for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR} and t_{KW} as needed to ensure that t_D is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

4.5.4. Ultra DMA

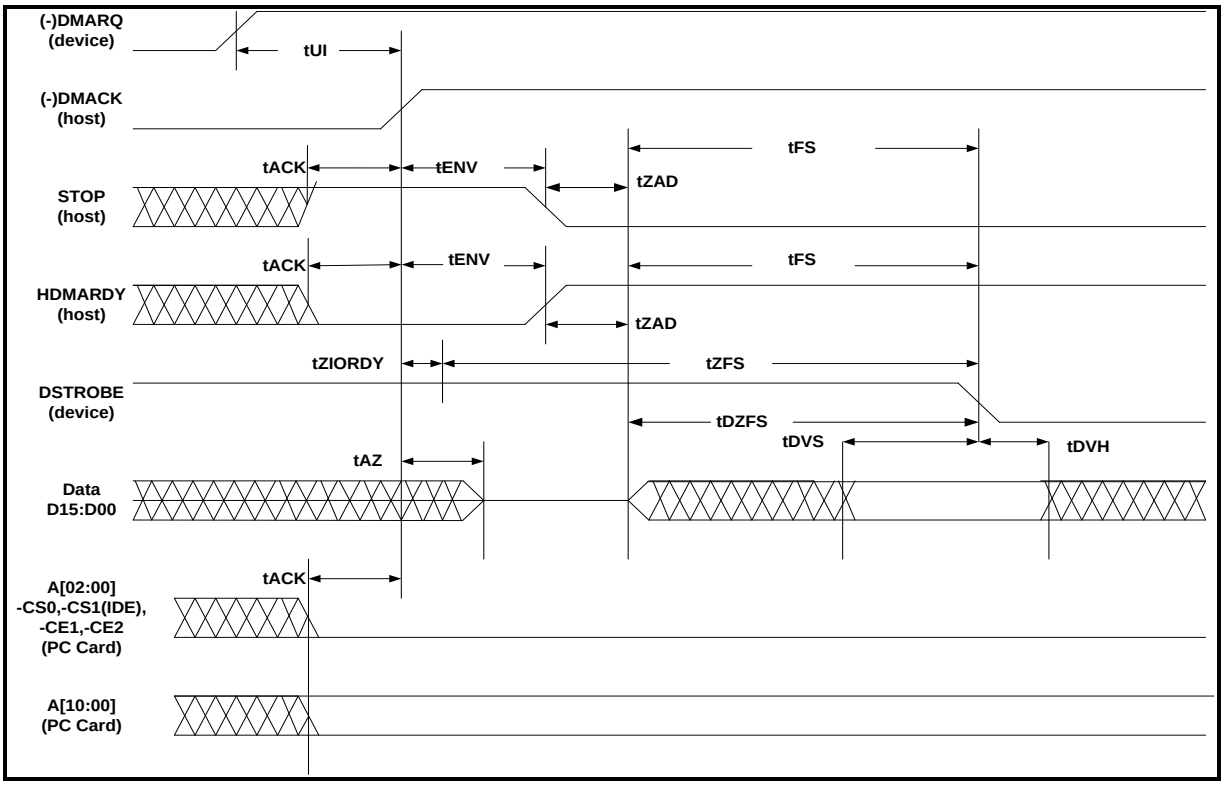


Figure 4-9 Initialize an Ultra DMA Data in Burst Timing

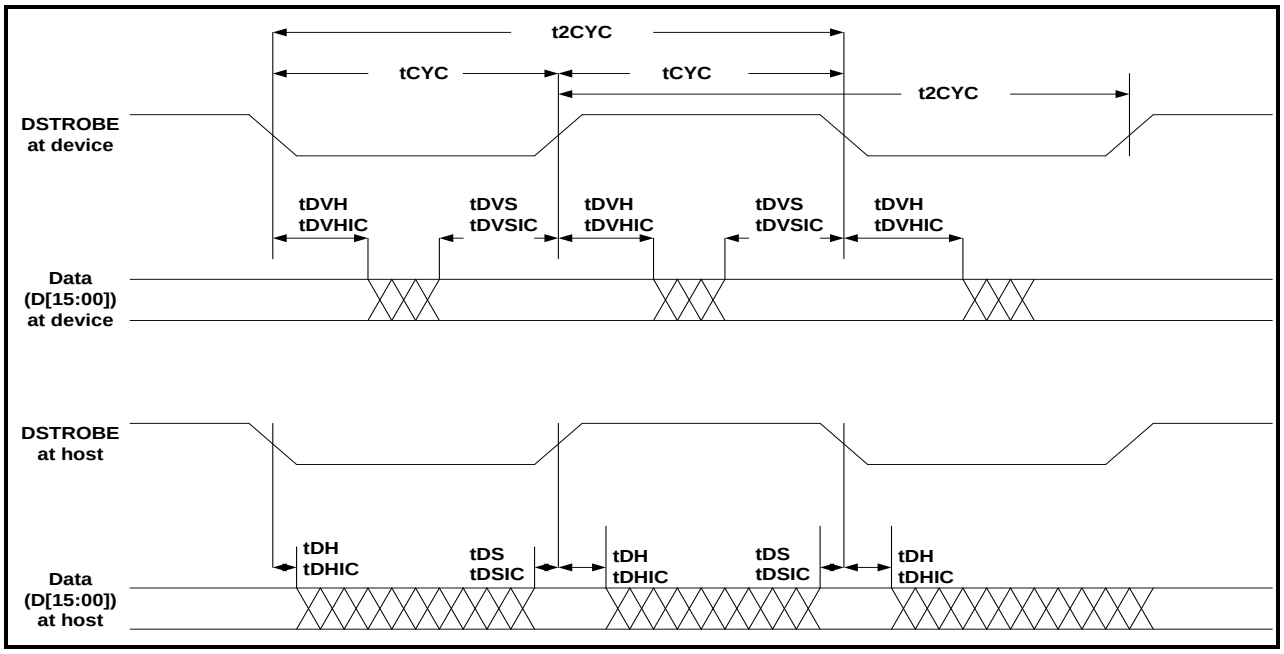


Figure 4-10 Sustained Ultra DMA Data-in Burst Timing

Table 4-10 Ultra DMA Mode Timing

	UDMA																Measure
Name	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Mode 6		Mode7		Location
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	(See Note 2)
t2CYCTYP	240		160		120		90		60		40		30		24		Sender
tCYC	112		73		54		39		25		16.8		13		10		Note 3
t2CYC	230		153		115		86		57		38		29		23		Sender
tDS	15		10		7		7		5		4		2.6		2.5		Recipient
tDH	5		5		5		5		5		4.6		3.5		2.9		Recipient
tDVS	70		48		31		20		6.7		4.8		4		2.9		Sender
tDVH	6.2		6.2		6.2		6.2		6.2		4.8		4		3.2		Sender
tCS	15		10		7		7		5		5		5		5		Device
tCH	5		5		5		5		5		5		5		5		Device
tCVS	70		48		31		20		6.7		10		10		10		Host
tCVH	6.2		6.2		6.2		6.2		6.2		10		10		10		Host
tZFS	0		0		0		0		0		35		25		15		Device
tDZFS	70		48		31		20		6.7		25		17.5		10.5		Sender
tFS		230		200		170		130		120		90		80		70	Device
tLI	0	150	0	150	0	150	0	100	0	100	0	75	0	60	0	50	Note 4
tMLI	20		20		20		20		20		20		20		20		Host
tUI	0		0		0		0		0		0		0		0		Host
tAZ		10		10		10		10		10		10		10		10	Note 5
tZAH	20		20		20		20		20		20		20		20		Host
tZAD	0		0		0		0		0		0		0		0		Device
tENV	20	70	20	70	20	70	20	55	20	55	20	50	20	50	20	50	Host
tRFS		75		70		60		60		60		50		50		50	Sender
tRP	160		125		100		100		100		85		85		85		Recipient
tIORDYZ		20		20		20		20		20		20		20		20	Device
tZI ORDY	0		0		0		0		0		0		0		0		Device
tACK	20		20		20		20		20		20		20		20		Host
tSS	50		50		50		50		50		50		50		50		Sender

Table 4-11 Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
t2CYCTYP	Typical sustained average two cycle time	
tCYC	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t2CYC	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
tDS	Data setup time at recipient (from data valid until STROBE edge)	2, 5
tDH	Data ho ld time at recipient (from STROBE edge until data may become invalid)	2, 5
tDVS	Data valid setup time at sender (from data valid until STROBE edge)	3
tDVH	Data valid ho ld time at sender (from STROBE edge until data may become invalid)	3
tCS	CRC word setup time at device	2
tCH	CRC word hold time device	2
tCVS	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
tCVH	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
tZFS	Time from STROBE output released-to-driving until the first transition of critical timing.	
tDZFS	Time from data output released-to-driving until the first transition of critical timing.	
tFS	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
tLI	Limited interlock time	1
tMLI	Interlock time with minimum	1
tUI	Unlimited interlock time	1
tAZ	Maximum time allowed for output drivers to release (from asserted or negated)	
tZAH	Minimum delay time required for output	
tZAD	drivers to assert or negate (from released)	
tENV	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK	
	to STOP during data outburst initiation)	
tRFS	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
tRP	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	

Name	Comment	Notes
tIORDYZ	Maximum time before releasing IORDY	6
tZI ORDY	Minimum time before driving IORDY	4, 6
tACK	Setup and ho ld times for -DMACK (before assertion or negation)	
tSS	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

NOTES:

1. The parameters t_{UI}, $t_{ML\ I}$, and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.
2. 80-conductor cabling shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.
3. Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
4. For all timing modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.
5. The parameters t_{DS} and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.
6. This parameter applies to True IDE mode operation only.

5. INTERFACE

5.1. Pin Assignment and Descriptions

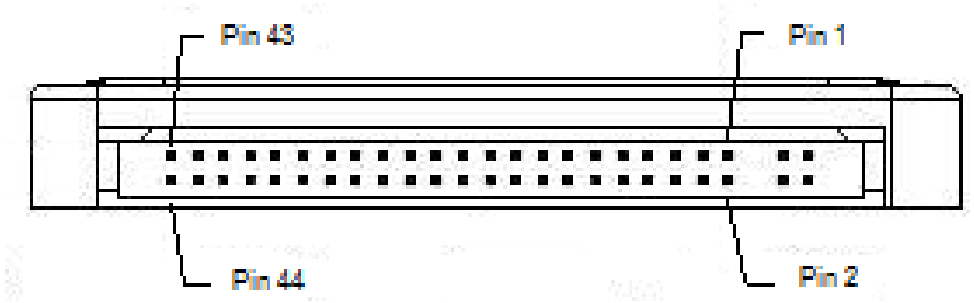


Table 5-1 2.5’’ PATA SSD Pin Assignments

Pin	Pin Name	Pin	Pin Name
01	-RESET	02	GND
03	DD7	04	DD8
05	DD6	06	DD9
07	DD5	08	DD10
09	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GND	20	KEY_PIN(OPEN)
21	DMARQ	22	GND
23	-DIOW:STOP	24	GND
25	-DIOR:-HDMARDY:HSTOBE	26	GND
27	IORDY:DDMARDY:DSTROBE	28	CSEL
29	-DMACK	30	GND
31	INTRQ	32	IOIS16
33	DA1	34	-PDIAG:-CBLID
35	DA0	36	DA2
37	-CS0	38	-CS1
39	-DASP	40	GND
41	VCC	42	VCC
43	GND	44	NC

Table 5-2 2.5’’ PATA SSD Pin Descriptions

Pin No.	Signal	I/O*	Description
01	-RESET	I	Hardware reset signal from the host
17,15,13,11,09,07, 05,03,04,06,08,10, 12,14,16,18	DD0~DD15(Device Data)	I/O	16-bit bi-direction Data Bus. DD (7:0) are used for 8-bit register transfers.
21	DMARQ(DMA Request)	O	For DMA data transfers. Device will assert DMARQ when the device is ready to transfer data to or from the host.
23	-DIOW(I/O Write)	I	This is the strobe signal used by the host to write to the device register or Data port
	STOP(Stop UDMA Burst)		The host assert this signal during an UDMA burst to stop the DMA burst
25	IORDY(I/O channel ready)	O	This signal is used to temporarily stop the host register access (read or write) when the device is not ready to respond to a data transfer request.
	DDMARDY(UDMA ready)		The device will assert this signal to indicate that the device is ready to receive UDMA data-out burst.
	DSTROBE(UDMA data strobe)		When UDMA mode DMA Read is active, this signal is the data-in strobe generated by the device.
28	CSEL(Cable select)	I	This pin is used to configure this device as Device 0 or Device 1.
29	-DMACK(DMA acknowledge)	I	This signal is used by the host in respond to DMARQ to initiate DMA transfer.
31	INTRQ(Interrupt)	O	When this device is selected, this signal is the active high Interrupt Request to the host
32	IOIS16	O	During PIO transfer mode0,1or 2, this pin indicates to the host the 16-bit data port has been addressed and the device is prepared to send or receive a 16-bit data word. When transferring in DMA mode, the host must use a 16-bit DMA channel and this signal will not be asserted.
35, 33, 36	DA0~DA2(Device Address)	I	This is 3-bit binary coded Address Bus.
34	-PDIAG(Passed diagnostics)	I/O	This signal will be asserted by Device 1 to indicate to Device 0 that Device 1 has completed diagnostics,

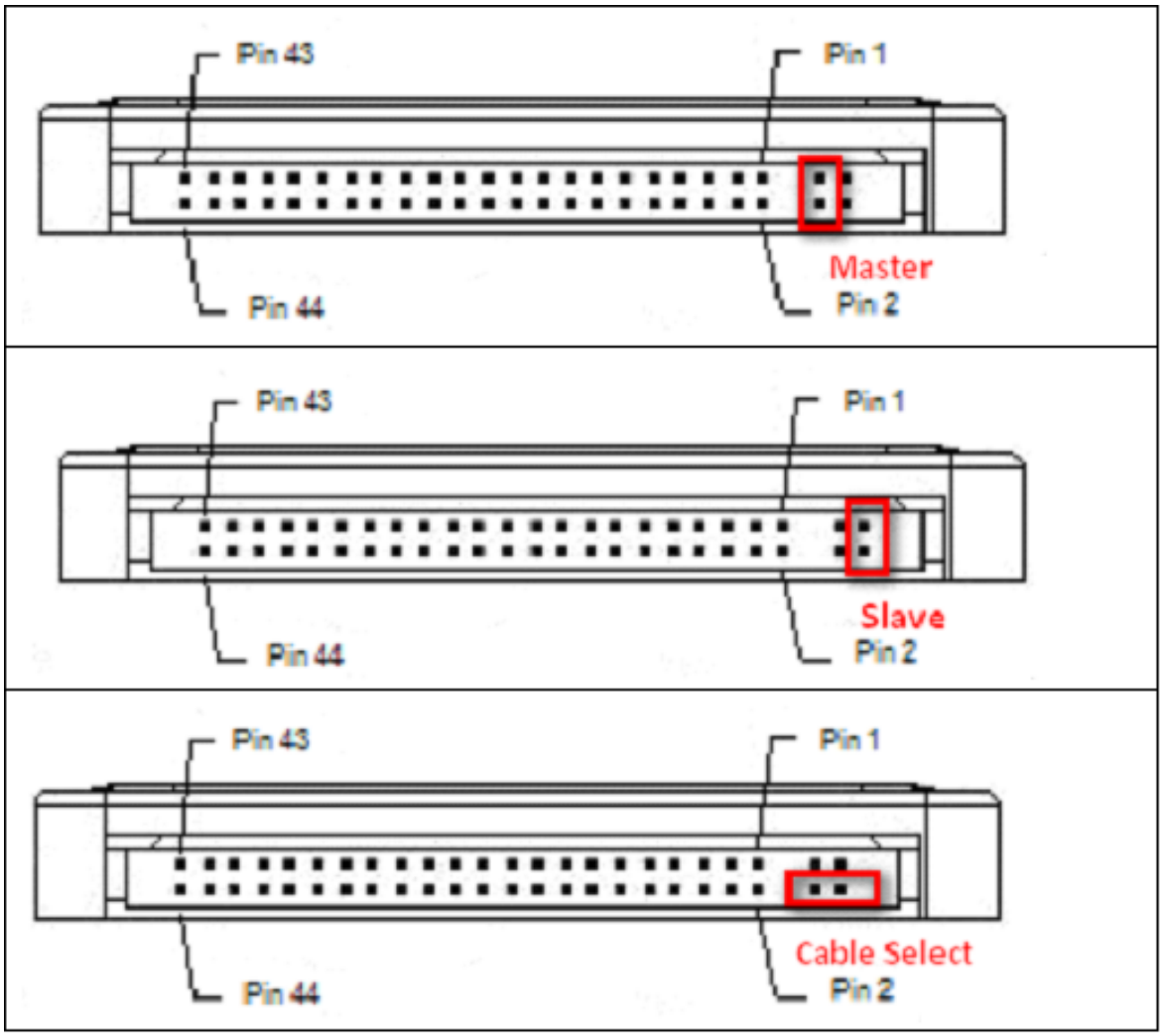
Pin No.	Signal	I/O*	Description
	-CBLID(Cable assembly type identify)		
37, 38	-CS0, -CS1(Chip select)	I	These signals are used to select the Command Block and Control Block registers. When –DMACK is asserted, -Cs0 and –Cs1 shall be negated and transfers shall be 16-bit wide.
39	-DASP(Device active, Device 1 present)	I/O	During the reset protocol, -DASP shall be asserted by Device 1 to indicate that the device is present.
41, 42	VCC	P	Power supply
02, 19, 22, 24, 26, 30, 40, 43	GND	--	Ground.

Note:

“I”	An input from the host system to the device
“O”	An output from the device to the host system
“I/O”	An input/output (bi-direction) common
“P”	Power supply

5.2. Jumper Setting

Following diagrams define 2.5” SSD Master/Slave Jumper settings.



6. SUPPORTED COMMANDS

6.1. Identify Drive Information

Table 6-1 List of Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848AH	2	General configuration bit-significant information
1	XXXX	2	Default number of cylinders
2	0000H	2	Reserved
3	XXXX	2	Default number of heads
4	0000H	2	Retired
5	0200H	2	Retired
6	XXXX	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card
9	0000H	2	Retired
10-19	XXXX	20	Serial Number in ASCII
20	0002H	2	Retired
21	0002H	2	Retired
22	0004H	2	Obsolete
23-26	XXXX	8	Firmware revision in ASCII
27-46	XXXX	40	Model number in ASCII
47	0001H	2	Maximum number of sector that shall be transferred on Read/Write Multiple commands
48	0000H	2	Reserved
49	0300H	2	Obsolete
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode 2
52	0000H	2	Retired
53	0007H	2	Word 54-58, 64-70 and 88 are valid
54	XXXX	2	Current numbers of cylinders
55	XXXX	2	Current numbers of heads
56	XXXX	2	Current sectors per track
57-58	XXXX	4	Current capacity in sectors (LBAs)(Word 57= LSW, Word 58= MSW)
59	0101H	2	Multiple sector setting is valid
60-61	XXXX	4	Total number of sectors addressable in LBA Mode

Word Address	Default Value	Total Bytes	Data Field Type Information
62	0000H	2	Retired
63	0007H	2	Multiword DMA mode 2 and below are supported
64	0003H	2	Advance PIO transfer modes supported
65	0078H	2	Minimum Multiword DMA transfer cycle time 120nsec
66	0078H	2	Manufacturer’s recommended Multiword DMA transfer cycle time 120nsec
67	0078H	2	Minimum PIO transfer cycle time without flow control 120nsec
68	0078H	2	Minimum PIO transfer cycle time with IORDY flow control 120nsec
69-81	0000H	26	Reserved
82	0002H	2	Supports Security Mode feature set
83-87	0000H	10	Reserved
88	0xxxH	2	Ultra DMA mode 7 and below are supported
89-127	0000H	78	Reserved
128	0021H	2	Enhanced security erase supported
129-159	0000H	62	Reserved vendor unique bytes
160-255	0000H	192	Reserved

6.2. CIS Information

Table 6-2 CIS Information

Address	Data	Description of Contents	CIS Function
000H	01H	CISTPL_DEVICE	Tuple code
002H	04H	TPL_LINK	Tuple link
004H	DFH	Device information	Tuple data
006H	4AH	Device information	Tuple data
008H	01H	Device information	Tuple data
00AH	FFH	END MARKER	End of Tuple
00CH	1CH	CISTPL_DEVICE_OC	Tuple code
00EH	04H	TPL_LINK	Tuple link
010H	02H	Conditions information	Tuple data
012H	D9H	Device information	Tuple data
014H	01H	Device information	Tuple data
016H	FFH	END MARKER	End of Tuple
018H	18H	CISTPL_JEDEC_C	Tuple code
01AH	02H	TPL_LINK	Tuple link
01CH	DFH	PCMCIA’s manufacturer’s JEDEC ID code	Tuple data
01EH	01H	PCMCIA’s JEDEC device code	Tuple data
020H	20H	CISTPL_MANFID	Tuple code
022H	04H	TPL_LINK	Tuple link
024H	0AH	Low byte of manufacturer’s ID code	Tuple data
026H	00H	High byte of manufacturer’s ID code	Tuple data
028H	00H	Low byte of product code	Tuple data
02AH	00H	High byte of product code	Tuple data
02CH	15H	CISTPL_VERS_1	Tuple code
02EH	13H	TPL_LINK	Tuple link
030H	04H	TPLLV1_MAJOR	Tuple data
032H	01H	TPLLV1_MINOR	Tuple data
034H	50H	‘ ’ (Vender Specific Strings)	Tuple data
036H	48H	‘ ’ (Vender Specific Strings)	Tuple data
038H	49H	‘ ’ (Vender Specific Strings)	Tuple data
03AH	53H	‘ ’ (Vender Specific Strings)	Tuple data
03CH	4FH	‘ ’ (Vender Specific Strings)	Tuple data

Address	Data	Description of Contents	CIS Function
03EH	4EH	‘ ’ (Vender Specific Strings)	Tuple data
040H	00H	Null Terminator	Tuple data
042H	43H	‘ ’ (Vender Specific Strings)	Tuple data
044H	46H	‘ ’ (Vender Specific Strings)	Tuple data
046H	20H	‘ ’ (Vender Specific Strings)	Tuple data
048H	43H	‘ ’ (Vender Specific Strings)	Tuple data
04AH	61H	‘ ’ (Vender Specific Strings)	Tuple data
04CH	72h	‘ ’ (Vender Specific Strings)	Tuple data
04EH	64H	‘ ’ (Vender Specific Strings)	Tuple data
050H	00H	Null Terminator	Tuple data
052H	00H	Reserved (Vender Specific Strings)	Tuple data
054H	FFH	END MARKER	End of Tuple
056H	21H	CISTPL_FUNCID	Tuple code
058H	02H	TPL_LINK	Tuple link
05AH	04H	IC Card function code	Tuple data
05CH	01H	System initialization bit mask	Tuple data
05EH	22H	CISTPL_FUNCE	Tuple code
060H	02H	TPL_LINK	Tuple link
062H	01H	Type of extended data	Tuple data
064H	01H	Function information	Tuple data
066H	22H	CISTPL_FUNCE	Tuple code
068H	03H	TPL_LINK	Tuple link
06AH	02H	Type of extended data	Tuple data
06CH	0CH	Function information	Tuple data
06EH	0FH	Function information	Tuple data
070H	1AH	CISTPL_CONFIG	Tuple code
072H	05H	TPL_LINK	Tuple link
074H	01H	Size field	Tuple data
076H	03H	Index number of last entry	Tuple data
078H	00H	Configuration register base address (Low)	Tuple data
07AH	02H	Configuration register base address (High)	Tuple data
07CH	0FH	Configuration register present mask	Tuple data
07EH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
080H	08H	TPL_LINK	Tuple link
082H	C0H	Configuration Index Byte	Tuple data

Address	Data	Description of Contents	CIS Function
084H	C0H	Interface Descriptor	Tuple data
086H	A1H	Feature Select	Tuple data
088H	01H	Vcc Selection Byte	Tuple data
08AH	55H	Nom V Parameter	Tuple data
08CH	08H	Memory length (256 byte pages)	Tuple data
08EH	00H	Memory length (256 byte pages)	Tuple data
090H	20H	Misc features	Tuple data
092H	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
094H	06H	TPL_LINK	Tuple link
096H	00H	Configuration Index Byte	Tuple data
098H	01H	Feature Select	Tuple data
09AH	21H	Vcc Selection Byte	Tuple data
09CH	B5H	Nom V Parameter	Tuple data
09EH	1EH	Nom V Parameter	Tuple data
0A0H	4DH	Peak I Parameter	Tuple data
0A2H	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0A4H	0AH	TPL_LINK	Tuple link
0A6H	C1H	Configuration Index Byte	Tuple data
0A8H	41H	Interface Descriptor	Tuple data
0AAH	99H	Feature Select	Tuple data
0ACH	01H	Vcc Selection Byte	Tuple data
0AEH	55H	Nom V Parameter	Tuple data
0B0H	64H	I/O Parameter	Tuple data
0B2H	F0H	IRQ parameter	Tuple data
0B4H	FFH	IRQ request mask	Tuple data
0B6H	FFH	IRQ request mask	Tuple data
0B8H	20H	Misc features	Tuple data
0BAH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0BCH	06H	TPL_LINK	Tuple link
0BEH	01H	Configuration Index Byte	Tuple data
0C0H	01H	Feature Select	Tuple data
0C2H	21H	Vcc Selection Byte	Tuple data
0C4H	B5H	Nom V Parameter	Tuple data
0C6H	1EH	Nom V Parameter	Tuple data
0C8H	4DH	Peak I parameter	Tuple data

Address	Data	Description of Contents	CIS Function
0CAH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0CCH	0FH	TPL_LINK	Tuple link
0CEH	C2H	Configuration Index Byte	Tuple data
0D0H	41H	Interface Descriptor	Tuple data
0D2H	99H	Feature Select	Tuple data
0D4H	01H	Vcc Selection Byte	Tuple data
0D6H	55H	Nom V Parameter	Tuple data
0D8H	EAH	I/O parameter	Tuple data
0DAH	61H	I/O range length and size	Tuple data
0DCH	F0H	Base address	Tuple data
0DEH	01H	Base address	Tuple data
0E0H	07H	Address length	Tuple data
0E2H	F6H	Base address	Tuple data
0E4H	03H	Base address	Tuple data
0E6H	01H	Address length	Tuple data
0E8H	EEH	IRQ parameter	Tuple data
0EAH	20H	Misc features	Tuple data
0ECH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0EEH	06H	TPL_LINK	Tuple link
0F0H	02H	Configuration Index Byte	Tuple data
0F2H	01H	Feature Select	Tuple data
0F4H	21H	Vcc Selection Byte	Tuple data
0F6H	B5H	Nom V Parameter	Tuple data
0F8H	1EH	Nom V Parameter	Tuple data
0FAH	4DH	Peak I Parameter	Tuple data
0FCH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
0FEH	0FH	TPL_LINK	Tuple link
100H	C3H	Configuration Index Byte	Tuple data
102H	41H	Interface Descriptor	Tuple data
104H	99H	Feature Select	Tuple data
106H	01H	Vcc Selection Byte	Tuple data
108H	55H	Nom V Parameter	Tuple data
10AH	EAH	I/O parameter	Tuple data
10CH	61H	I/O range length and size	Tuple data
10EH	70H	Base address	Tuple data

Address	Data	Description of Contents	CIS Function
110H	01H	Base address	Tuple data
112H	07H	Address length	Tuple data
114H	76H	Base address	Tuple code
116H	03H	Base address	Tuple link
118H	01H	Address length	Tuple data
11AH	EEH	IRQ parameter	Tuple data
11CH	20H	Misc features	Tuple data
11EH	1BH	CISTPL_CFTABLE_ENTRY	Tuple code
120H	06H	TPL_LINK	Tuple link
122H	03H	Configuration Index Byte	Tuple data
124H	01H	Feature Select	Tuple data
126H	21H	Vcc Selection Byte	Tuple data
128H	B5H	Nom V Parameter	Tuple data
12AH	1EH	Nom V Parameter	Tuple data
12CH	4DH	Peak I Parameter	Tuple data
12EH	14H	CISTPL_NO_LINK	Tuple code
130H	00H	TPL_LINK	Tuple link
132H	FFH	CISTPL_END	End of Tuple
134H	FFH	CISTPL_END	End of Tuple
136H	FFH	CISTPL_END	End of Tuple
138H	FFH	CISTPL_END	End of Tuple
13AH	FFH	CISTPL_END	End of Tuple

7. ACRONYMS

Term	Definitions
LBA	Logical block addressing
MB	Mega-byte
MTBF	Mean time between failures
PATA	Parallel advanced technology attachment
S.M.A.R.T.	Self-monitoring, analysis and reporting technology
SSD	Solid state drive

8. PART NUMBER DECODER

PFD-2ACX^{1}X^{2}X^{3}X^{4}X^{5}X^{6}X^{7}X^8

Item	Size	Series	Capacity	NAND Flash & Temperature Grade	Mode	Option
			X^1 X^2 X^3 X^4	**X^5**	**X^6**	**X^{7}X^8**
PFD	**2**	**AC**	**256M** (256MB) **512M** (512MB) **001G** (1GB) **002G** (2GB) **004G** (4GB) **008G** (8GB) **016G** (16GB) **032G** (32GB) **064G** (64GB) **128G** (128GB) **256G** (256GB)	**C** : SLC , Standard (0°C ~ +70°C) **I** : SLC , Wide (-40°C ~ +85°C) **K** : MLC , Standard (0°C ~ +70°C) **M** : MLC , Wide (-40°C ~ +85°C)	See below	See below

X^6 (Data Transfer Mode / Disk Mode)

P: PIO mode / Fixed disk mode

M: MWDMA mode / Fixed disk mode

U: UDMA mode / Fixed disk mode

X^{7}X^8 [Reserved for specific requirement]

Blank: standard