Amtron Technology, Inc.

Industrial Grade M.2 2280 PCIe SSD

AH Series

Product Datasheet

V1.2

Table of Contents

1. INTRODUCTION

1.1. Description

Amtron industrial AH series M.2 2280 PCIe SSD is designed with PCIe Gen4 x4 interface and is fully compliant with the standard Next Generation Form Factor (NGFF). It can reach up to 7200 MB/s read and 6800 MB/s write high performance based on 112Layers 3D TLC NAND flash with the choice of 512MB/1GB/2GB DDR4. These M.2 PCIe modules are offered in standard temperature grade (0°C to +70°C) and wide temperature grade (-40°C to +85°C). The memory capacities are available from 480GB to 7680GB.

1.2. Product Features

- M.2 2280-D2-M-H2 form factor
- PCI Express Base Version 4.0 and Compliant with NVMe 1.4
- PCIe Gen4 x 4 lane & backward compatible to PCIe Gen3, Gen2 and Gen1
- RoHS compliant [Lead free]
- 3D Triple Level Cell (TLC) NAND Flash
- Capacity from 480GB up to 7680GB
- High speed:
  Read 7,200 MB/s max., Write 6,800 MB/s max.
- Endure severe thermal and dynamic environments
- Very low power consumption
- MTBF > 1.500,000 hours *
- Support SMART and TRIM Command
- Controlled Bill of Materials (BOM)

***Note**: Lower MTBF is expected for higher capacity drives. To be conservative, the lowest MTBF is reported in this document

1.3. Product Overview

- **Capacity**
  - 480GB up to 7,680GB
- **Form Factor**
  - E18 M.2 2280-D2-M-H2
- **PCIe Interface**
  - PCIe Gen4 x4
  - NVMe 1.4
  - PCI Express Base 4.0
- **Flash Interface**
  - 480GB = 128GB (DDP) x 4pcs
  - 960GB = 256GB (QDP) x 4pcs
  - 1,920GB = 512GB (ODP) x 4pcs
    = 256GB (QDP) x 8pcs
  - 3,840GB = 1TB (ODP) x 4pcs
    = 512GB (ODP) x 8pcs
  - 7,680GB = 1TB (ODP) x 8pcs
- **Performance[1]**
  - **With SLC cache**
    - Seq. Read up to 7,200 MB/s
    - Seq. Write up to 6,800 MB/s
    - Ran. 4K Read up to 1,000K IOPS
    - Ran. 4K Write up to 1,000K IOPS
  - **Without SLC cache**
    - Seq. Read up to 7,000 MB/s
    - Seq. Write up to 2,200 MB/s
    - Ran. 4K Read up to 800K IOPS
    - Ran. 4K Write up to 500K IOPS
- **Temperature Range[2]**
  - Operation Temperature:
    - Standard: 0°C ~ 70°C
    - Wide: -40°C ~ 85°C
  - Storage Temperature:
    - -40°C ~ 85°C
- **ECC**
  - LDPC / RAID ECC
  - Low density parity check code
    (>120buit/KBytes)
- **Power Consumption[3]**
  - Active Write (Max.): < 12W
  - Active Read (Max.): < 12W
  - Idle mode: < 3W
- **Reliability**
  - MTBF[4]: 1.5 million hours
  - UBER[5]: < 1 sector per 10^{16} bits
  - DWPD ≥ 1.5
  - TBW: 480GB: 770TB
    960GB: 1,660 TB
    1,920GB: 3,400 TB
    3,840GB: 6,800 TB
    7,680GB: 13,600 TB
- **Environment Specification**
  - Shock: $1500G_{0\text{-}P}$/0.5ms duration
  - Vibration: 20Hz~80Hz/1.52mm
    80Hz~2000Hz/$20G_{P\text{-}P}$
  - Drop: 80cm height/each face
  - Conflicting Material: Concrete floor
- **RoHS Compliant**
- **EMI Compliant**
  - EN55032, CISPR 32 (CE)
  - AS/NZS CISPR 32 (CE)
  - ANSI C63.4 (FCC)
  - CNS 13438 (BSMI)
  - VCCI-CISPR 32 (VCCI)
- **Features Support List**
  - TCG Pyrite/OPAL
  - Write Protect
  - Secure Erase (Quick Erase)

Notes:

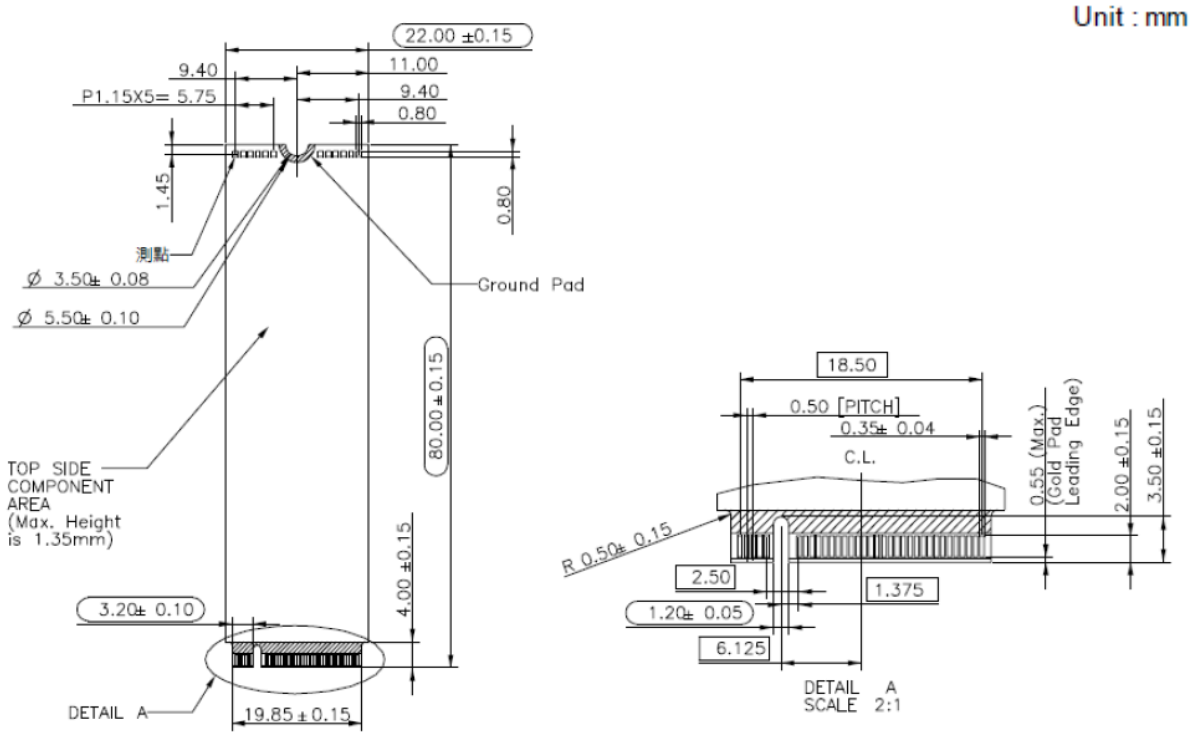
1. Refer to Chapter 2.3 for more details.
2. The operation temperature means the case temperature, in which can be detected via the S.M.A.R.T. Operation temperature range depends on NAND flash applied capability, which maximum value is listed.
3. Refer to Section 4.2 power consumption for more details.
4. Mean Time Between Failure (MTBF)
5. Uncorrectable Bit Error Rate (UBER)

1.4. Product Dimension

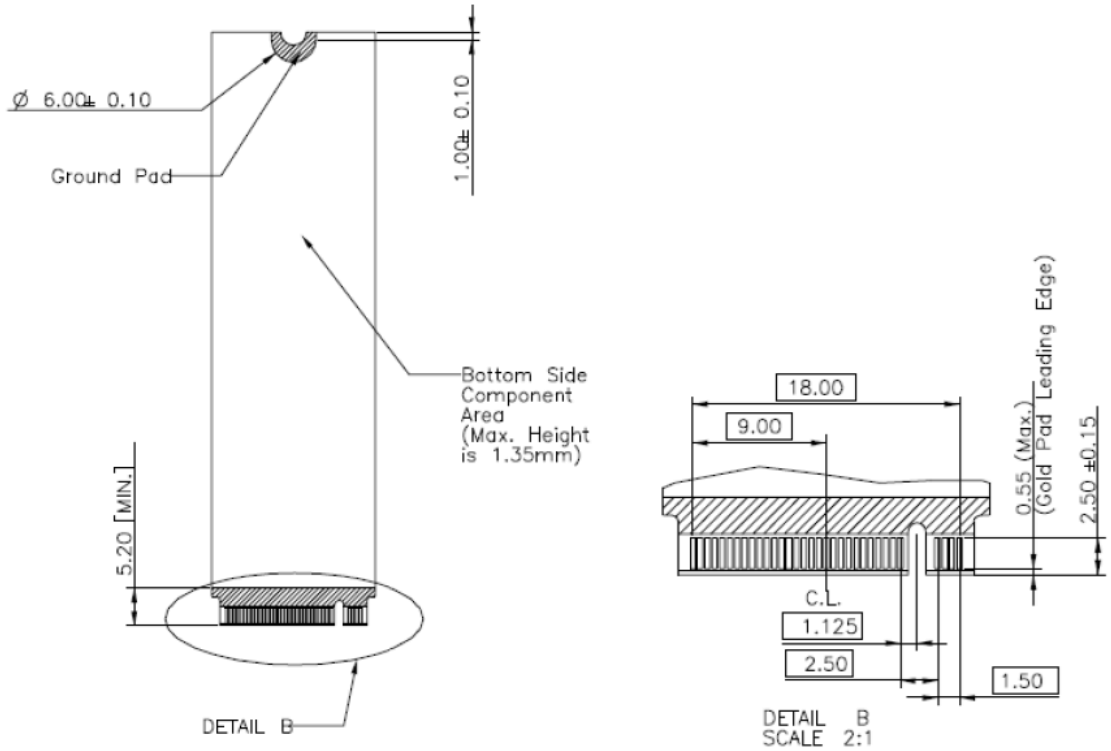
- **Dimension of M.2 2280-D2-M: 80mm(L) x 22mm(W) x 3.5mm(H)**

Top View

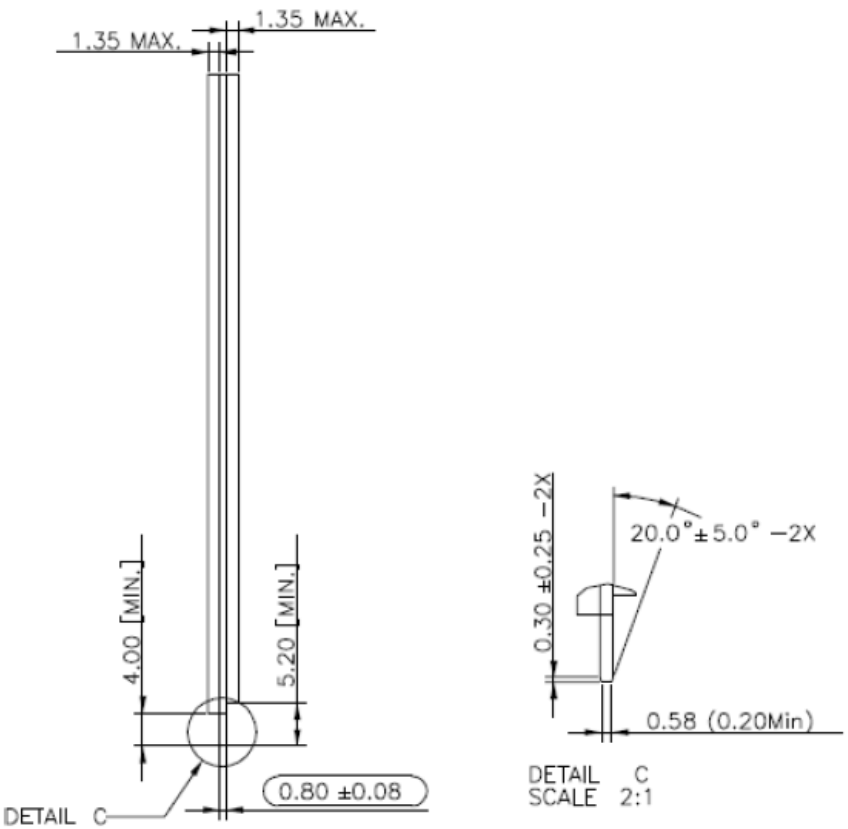
Unit : mm



Bottom View



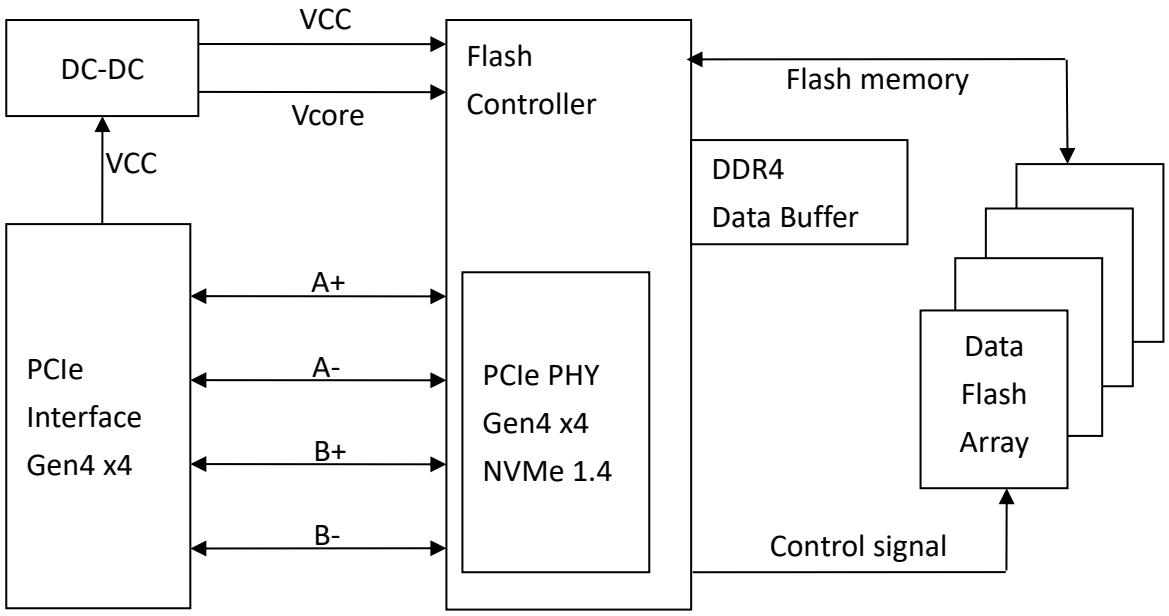
Side View



***Notes:**

1. General Tolerance: ±0.15mm
2. ⬭ is IQC inspection dimension

1.5. Block Diagram



M.2 2280 PCIe SSD Block Diagram

2. PRODUCT SPECIFICATIONS

2.1. Specifications

- **Capacity**
  - 480GB up to 7,680GB
- **Electrical/Physical Interface**
  - PCIe Interface
  - PCI Express Base Ver 4.0
  - Compliant with NVMe 1.4
  - PCIe Gen4 x 4 lane & backward compatible to PCIe Gen3, Gen2 and Gen1

2.2. Device Capacity

Capacity	IDEMA Standard		User Data Size
	512Bytes/Sector	4KBytes/Sector	
	Total Sectors (LBA)	Total Sectors (LBA)	
480GB	937,703,088	117,212,886	Depended on file management
960GB	1,875,385,008	234,423,126	
1,920GB	3,750,748,848	468,843,606	
3,840GB	7,501,476,528	937,684,566	
7,680GB	15,002,931,888	1,875,366,486	

Notes:

1. 1 Gigabyte (GB) is equal to 1,000,000,000 Bytes; 1 sector is equal to 512 Bytes or 4K Bytes.
2. The calculation is following IDEMA Standard.
3. The total actual user data size of the SSD may be less than device capacity due to SSD format, SSD partition, operating system.

   EX: OS shows 447.13GB (NTFS) on 480GB device.

2.3. Performance

- **Sequential Performance with Commercial Temperature Flash (MB/s)**

Capacity	Flash Structure	Sequential (MB/s) (With SLC cache)[1]		Sequential (MB/s) (Direct TLC)	
		Read	Write	Read	Write
480GB	128GB x4, BGA BiCS5 112Layers	6,500	4,000	4,000	350
960GB	256GB x4, BGA BiCS5 112Layers	7,200	6,300	7,000	750
1,920GB	512GB x4, BGA BiCS5 112Layers	7,200	6,500	7,000	1,500
3,840GB	1TB x4, BGA BiCS5 112Layers	7,200	6,300	7,000	1,000
	512GB x8, BGA BiCS5 112Layers	7,000	6,800	6,500	2,200
7,680GB	1TB x8, BGA BiCS5 112Layers	7,000	6,800	6,600	2,000

- **Sequential Performance with Wide Temperature Flash (MB/s)**

Capacity	Flash Structure	Sequential (MB/s) (With SLC cache)[1]		Sequential (MB/s) (Direct TLC)	
		Read	Write	Read	Write
480GB	128GB x4, BGA BiCS5 112Layers	6,400	2,400	4,000	340
960GB	256GB x4, BGA BiCS5 112Layers	7,200	4,800	7,000	750
1,920GB	512GB x4, BGA BiCS5 112Layers	7,200	6,300	7,000	1,200
	256GB x8, BGA BiCS5 112Layers	7,000	6,400	6,800	1,500
3,840GB	512GB x8, BGA BiCS5 112Layers	7,000	6,800	6,600	2,200

Notes:

1. Adopts dynamic caching to deliver better performance and consumer user experience.
2. Performance may differ according to flash configuration, use condition, environment and platform.
3. Performance specification is under Thermal Throttling inactivated.
4. Tested with CrystalDiskMark 7.0, QD128T1, 1GB range.
5. Operating System: Windows 10 Professional (x64); Intel Core i7-8700K CPU @ 3.70GHz
6. Measurement environment: Room temperature: 20~25℃, humidity: 40~60%RH, DC+3.3V condition.

- **Random Performance with Commercial Temperature Flash (IOPS)**

Capacity	Flash Structure	Random (IOPS) (With SLC cache)[1]		Random (IOPS) (Direct TLC)	
		Read	Write	Read	Write
480GB	128GB x4, BGA BiCS5 112Layers	450K	700K	230K	90K
960GB	256GB x4, BGA BiCS5 112Layers	750K	1,000K	480K	190K
1,920GB	512GB x4, BGA BiCS5 112Layers	1,000K	1,000K	800K	380K
3,840GB	1TB x4, BGA BiCS5 112Layers	950K	1,000K	580K	200K
	512GB x8, BGA BiCS5 112Layers	870K	1,200K	850K	500K
7,680GB	1TB x8, BGA BiCS5 112Layers	1,500K	1,200K	850K	470K

- **Random Performance with Wide Temperature Flash (IOPS)**

Capacity	Flash Structure	Random (IOPS) (With SLC cache)[1]		Random (IOPS) (Direct TLC)	
		Read	Write	Read	Write
480GB	128GB x4, BGA BiCS5 112Layers	220K	605K	125K	85K
960GB	256GB x4, BGA BiCS5 112Layers	450K	1,000K	270K	180K
1,920GB	512GB x4, BGA BiCS5 112Layers	520K	1,000K	380K	240K
	256GB x8, BGA BiCS5 112Layers	640K	1,200K	520K	380K
3,840GB	512GB x8, BGA BiCS5 112Layers	540K	1,200K	540K	500K

Notes:

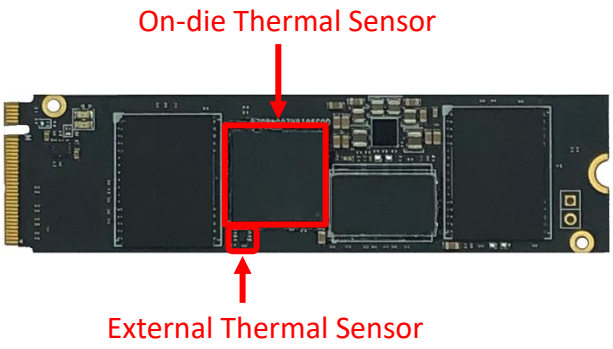
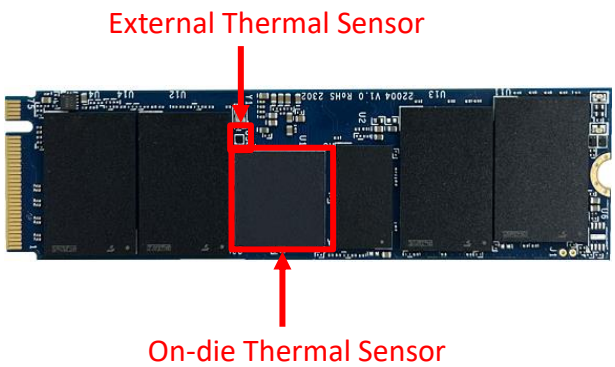
1. Adopts dynamic caching to deliver better performance and consumer user experience.
2. Performance may differ according to flash configuration, use condition, environment and platform.
3. Performance specification is under Thermal Throttling inactivated.
4. Tested with IOMeter, 1GB range, 4K data size, QD=128, 16 worker, 4k aligned
5. Operating System: Windows 10 Professional (x64); Intel Core i7-8700K CPU @ 3.70GHz
6. Measurement environment: Room temperature: 20~25℃, humidity: 40~60%RH, DC+3.3V condition.

2.4. Thermal Throttling

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. The controller is designed with an on-die thermal sensor and with its accuracy, firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via S.M.A.R.T. reading.

- **Purpose of Thermal Throttling:**
  - In order to keep the optimal performance in the safe range of the temperature.

- **Thermal sensors:**
  - We have external thermal sensor & on-die thermal sensor (internal controller) to detect temperature. There is 1pcs external thermal sensor on PCB, the position depends on different form factor (The thermal sensor is shown below. The picture is for reference only).
  - External thermal sensor would detect flash temperature; On-die thermal sensor detect controller temperature.

Type1: 4x NAND PCBA (Top Side)	Type2: 8x NAND PCBA (Top Side)
	

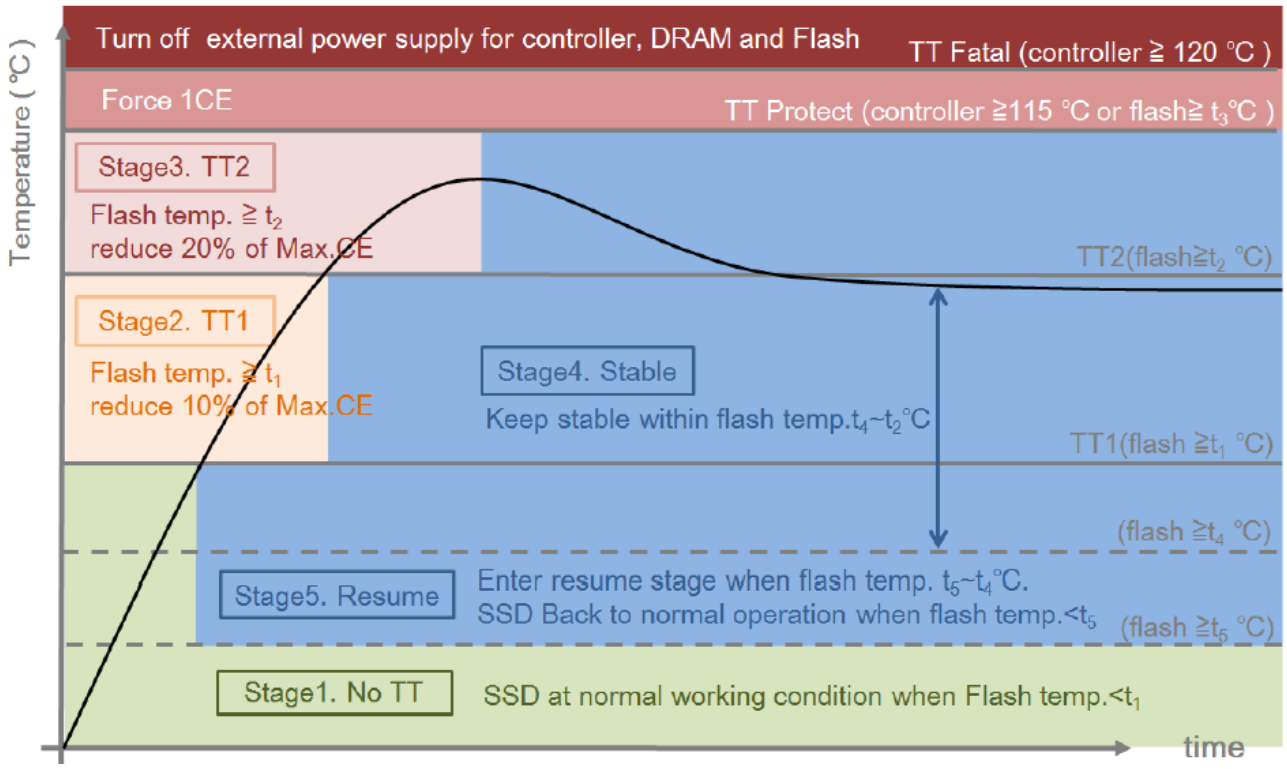


Figure 2-1 Thermal Throttling Schematic

	Operation temp. of Normal-temp. grade: 0°C ~ 70°C	Operation temp. of Wide-temp. grade: -40°C ~ 85°C
t_1	68°C	82°C
t_2	70°C	85°C
t_3	80°C	95°C
t_4	64°C	78°C
t_5	60°C	74°C

Notes:

1. TT shown on Figure 2-1 means “Thermal Throttling”.
2. CE = Chip Enable.
3. temp. = temperature

2.5. TCG Opal 2.0

The Opal specification is a set of specifications for self-encrypting drives published by the Trusted Computing Group (TCG), a non-profit organization that develops, defines, and promotes standards and specifications for secure computing. The Opal Security Subsystem Class(SSC) 2.0 defines the details of data management in storage devices and the classes authority for data access, and secures data from theft and tampering by unauthorized persons who are able to gain access to the storage device or host system.

TCG Opal 2.0 Main Features:

- AES 256-bit Hardware Self Encryption
- Deploy Storage Device & Take Ownership:

  The Storage Device is integrated into its target system and ownership transferred by setting or changing the Storage Device's owner credential.
- Activate or Enroll Storage Device:

  LBA ranges are configured and data encryption and access control credentials (re)generated and/or set on the Storage Device. Access control is configured for LBA range unlocking.
- Lock & Unlock Storage Device:

  Unlocking of one or more LBA ranges by the host and locking of those ranges under host control via either an explicit lock or implicit lock triggered by a reset event. MBR shadowing provides a mechanism to boot into a secure pre-boot authentication environment to handle device unlocking.
- Repurpose & End-of-Life:

  Erasure of data within one or more.
- Physical Presence SID (PSID):

  PSID is defined by TCG OPAL as a 32-character string and the purpose is to revert SSD back to its manufacturing setting when the drive is still OPAL-activated. PSID code can be printed on a SSD label when an OPAL-activated SSD supports PSID revert feature.

2.6. TBW (TeraBytes Written) and DWPD (Drive Write Per Day)

Capacity	Flash Type	TBW	DWPD
480GB	128GB x4, BGA BiCS5 112Layers	770	1.4
960GB	256GB x4, BGA BiCS5 112Layers	1,660	1.5
1,920GB	512GB x4, BGA BiCS5 112Layers 256GB x8, BGA BiCS5 112Layers	3,400	1.6
3,840GB	1TB x4, BGA BiCS5 112Layers 512GB x8, BGA BiCS5 112Layers	6,800	1.6
7,680GB	1TB x8, BGA BiCS5 112Layers	13,600	1.6

Notes:

1. TBW is measured by JEDEC Client 219A workload and calculated with PE count = 3000.
2. TBW may differ according to flash configuration and platform.
3. DWPD is calculated based on 3-year lifetime.
4. DWPD = TBW / (365 x 3years x User capacity)
5. The SSD supports trim function. If Operation System does not support trim command, performance and TBW will be affected. (Like certain Windows OS, Linux kernel version before 2.6.33, other OS please reference each own user manual)
6. The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor.

2.7. UBER

Capacity	UBER
480GB ~7,680GB	< 1 sector per 10^{16} bits read

Notes:

1. UBER (Uncorrectable Bit Error Rates) means the uncorrectable error per bits read.
2. UBER = FER (fail rate) / Data Size (user data bit).
3. FER = uncorrectable ECC frame number / total ECC frame number.
4. The LDPC for TLC ECC capability > 120bit/KB.

2.8. MTBF

MTBF (mean time between failures) is a measure of how reliable a hardware product is. Its value represents the average time between a failure repair and the next failure. The unit of MTBF is typically in hours. The higher the MTBF value, the higher the reliability of the product. Please note that a lower MTBF is expected for higher capacity drives. To be conservative, the lowest MTBF is reported in this document. The MTBF calculated in this document is based on a software tool, Relex 7.3 . The predicted MTBF for Amtron AH series M.2 PCIe SSD is >1,500,000 hours

Capacity	MTBF
480GB ~ 7,680GB	1.5 million hours

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

	Mode	Min.	Max.	Unit
Temperature Ranges	Operation (Standard)	0	70	℃
	Operation (Wide)	-40	85	℃
	Storage	-40	85	℃
Humidity	Operation	5	95	%
	Storage	5	95	%
Temperature Cycle Test	Operation (Standard)	0	70	℃
	Operation (Wide)	-40	85	℃
	Storage	-40	85	℃

Notes:

1. The operation temperature means the case temperature, in which can be detected via the S.M.A.R.T. Airflow is suggested and it will allow device to be operated at appropriate temperature for each component during heavy workloads environment.

3.1.2. Mechanical Specification

Items			Condition
Shock	Non-operational	Acceleration Force	1500G 0-p with half sine wave (0.5ms)
Vibration	Non-operational	Frequency/Displacement	20Hz~80Hz/1.52mm
		Frequency/Acceleration	80Hz~2000Hz/20G p-p with sine wave
Drop	Non-operational	Height of Drop	80cm free fall
		Number of Drop	6 face of each unit
		Conflicting Material	Concrete floor

3.1.3. Electrostatic Discharge (ESD)

Specification	+/- 4KV
EN 55024, CISPR 24 EN 61000-4-2 and IEC 61000-4-2	Device functions are affected, but EUT will be back to its normal or operational state automatically.

3.1.4. EMI Compliance

Specification
EN 55032, CISPR 32 (CE)
AS/NZS CISPR 32 (CE)
ANSI C63.4 (FCC)
VCCI-CISPR 32 (VCCI)
CNS 13438 (BSMI)

3.2. Certification & Compliance

- RoHS
- ISO 9001
- ISO 14001
- ISO 45001
- ISO 27001

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Parameter	Rating
Operating Voltage	3.3V ± 5%
Rise Time (Max/Min)	100ms / 0.1ms
Fall Time (Max/Min)	5s / 10ms
Min. off Time[Note1]	1s

Notes:

1. Minimum time between power removed from SSD (Vcc < 100 mV) and power re-applied to the drive.
2. Ensure the voltage of each power domain in SSD has enough time to discharge less than 0.1V.
3. Rise Time during from 10% to 90% of 3.3V.
4. Fall Time during from 90% to 10% of 3.3V.

4.2. Power Consumption

Capacity	Flash Structure	SLC cache on		SLC cache off		Idle
		Read	Write	Read	Write	
480GB	128GB x4, BGA BiCS5 112Layers	8.8	7.5	6.5	4.5	2
960GB	256GB x4, BGA BiCS5 112Layers	10.1	9.5	9.7	6	2
1,920GB	512GB x4, BGA BiCS5 112Layers	10.6	10.5	10.3	8.2	2
	256GB x8, BGA BiCS5 112Layers	10.8	10.7	10.5	8.5	2.7
3,840GB	1TB x4, BGA BiCS5 112Layers	10.9	11	10.8	7.8	2
	512GB x8, BGA BiCS5 112Layers	11	11.3	11.1	11.8	2.7
7,680GB	1TB x8, BGA BiCS5 112Layers	11.2	11.1	11.5	11.9	2.8

Unit: W

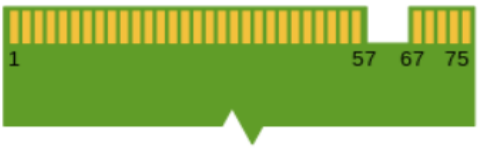
Notes:

1. Use CrystalDiskMark 7.0.0 with the setting of 1GB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5].
2. Power consumption may differ according to flash configuration, use condition, environment and platform.
3. The measured power voltage is 3.3V.
4. Measurement environment: Room temperature: 20~25℃, humidity: 40~60%RH, DC+3.3V condition.

5. INTERFACE

5.1. Pin Assignment and Descriptions

The follow table defines the signal assignment of the internal NGFF connector for SSD usage, described in the PCI Express M.2 Specification version 1.1 of the PCI-SIG.



Pin #	SATA Pin	Description
1	GND	Ground
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	No connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	N/C	No connect
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
Pin #	**SATA Pin**	**Description**

24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	N/C	No connect
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform.
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pull-up on platform.
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#(O)(0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active low.
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.

Pin #	SATA Pin	Description
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	N/C	No Connect Reserve for Quick Erase; Low active.
68	N/C	No Connect
69	N/C	PEDET (NC-PCIe). No Connect for PCIe.
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	Ground

6. SUPPORTED COMMANDS

6.1. NVMe Command List

Table 6-1 Admin Commands

Identifier	O/M	Command Description
00h	M	Delete I/O Submission Queue
01h	M	Create I/O Submission Queue
02h	M	Get Log Page
04h	M	Delete I/O Completion Queue
05h	M	Create I/O Completion Queue
06h	M	Identify
08h	M	Abort
09h	M	Set Features
0Ah	M	Get Features
0Ch	M	Asynchronous Event Request
10h	O	Firmware Activate
11h	O	Firmware Image Download
14h	O	Device Self-test
80h	O	Format NVM
81h	O	Security Send
82h	O	Security Receive
84h	O	Sanitize

Table 6-2 I/O Commands

Identifier	O/M	Command Description
00h	O	Flush
01h	O	Write
02h	O	Read
04h	O	Write Uncorrectable
05h	O	Compare
08h	O	Write Zeroes
09h	O	Dataset Management

Table 6-3 Set Feature Commands

Identifier	O/M	Command Description
00h		Reserved
01h	M	Arbitration
02h	M	Power Management
03h	O	LBA Range Type
04h	M	Temperature Threshold
05h	M	Error Recovery
06h	O	Volatile Write Cache
07h	M	Number of Queues
08h	M	Interrupt Coalescing
09h	M	Interrupt Vector Configuration
0Ah	M	Write Atomicity Normal
0Bh	M	Asynchronous Event Configuration
0Ch	O	Autonomous Power State Transition
0Dh	O	Host Memory Buffer
0Eh	O	Timestamp
10h	O	Host Controlled Thermal Management
11h	O	Non-Operational Power State Config
0Eh – 7Dh		Reserved
80h	O	Software Progress Marker

Table 6-4 Get Log Page Commands

Identifier	O/M	Command Description
00h		Reserved
01h	M	Error Information
02h	M	SMART / Health Information
03h	M	Firmware Slot Information
04h	O	Changed Namespace List
06h	O	Device Self-test
09h – 7Fh		Reserved
81h	O	Sanitize Status
82h - FFh		Reserved

6.2. Identify Device Command

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 6-5 Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	TBD
63:24	M	Model Number (MN)	TBD
71:64	M	Firmware Revision (FR)	TBD
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M	IEEE OUI Identifier (IEEE)	0x6479A7
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x09
79:78	M	Controller ID (CNTLID)	0x0001
83:80	M	Version (VER)	0x00010300
87:84	M	RTD3 Resume Latency (RTD3R)	0x00989680
91:88	M	RTD3 Entry Latency (RTD3E)	0x00989680
95:92	M	Optional Asynchronous Events Supported (OAES)	0x00000200
99:96	M	Controller Attributes (CTRATT)	0x0002
101:100	O	Read Recovery Level support bitmap (RRLS)	0x00
110:102	-	Reserved	0x00
111	M	Controller Type, if support NVMe 1.4 shall be set to other than 0 (cntrltype)	0x00
127:112	O	FRU Globally Unique Identifier (FGUID[16])	0x00
129:128	O	Command Retry Delay Time 1 (CRDT1)	0x00
131:130	O	Command Retry Delay Time 2 (CRDT2)	0x00
133:132	O	Command Retry Delay Time 3 (CRDT3)	0x00
255:134	-	Reserved	0x00
257:256	M	Optional Admin Command Support (OACS)	0x0017
258	M	Abort Command Limit (ACL)	0x03
259	M	Asynchronous Event Request Limit (AERL)	0x03
260	M	Firmware Updates (FRMW)	0x12
261	M	Log Page Attributes (LPA)	0x08
262	M	Error Log Page Entries (ELPE)	0x3E
Bytes	**O/M**	**Description**	**Default Value**

263	M	Number of Power States Support (NPSS)	0x00
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x00
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x015C
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x0161
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x0064
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x00000000
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x00000000
295:280	O	Total NVM Capacity (TNVMCAP)	**
311:296	O	Unallocated NVM Capacity (UNVMCAP)	**
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00
317:316	O	Extended Device Self-test Time (EDSTT)	0x000A
318	O	Device Self-test Options (DSTO)	0x00
319	M	Firmware Update Granularity (FWUG)	0x01
321:320	M	Keep Alive Support (KAS)	0x0000
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	0x0001
325:324	O	Minimum Thermal Management Temperature (MNTMT)	0x0139
327:326	O	Maximum Thermal Management Temperature (MXTMT)	0x0166
331:328	O	Sanitize Capabilities (SANICAP)	0x07
335:332	O	Host Memory Buffer Min. Descriptor Entry Size (hmminds)	0x00
337:336	O	Host Memory Maximum Descriptor Entries (hmmaxd)	0x00
339:338	O	NVM Set ID Maximum (nsetidmax)	0x00
341:340	O	Endurance Group ID Maximum (endgidmax)	0x00
342	O	ANA Maximum Transition Time (anatt)	0x00
343	O	Asymmetric Namespace Access Capabilities (ANACAP)	0x00
347:344	O	ANA Group ID Maximum (anagrpmax)	0x00
Bytes	**O/M**	**Description**	**Default Value**
351:348	O	Number of ANA Group IDs (nanagrpid)	0x00

355:352	O	Persistent Event Log Size (PELS)	0x00
511:356	-	Reserved	0x00
NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	M	Maximum Outstanding Commands (MAXCMD)	0x0100
519:516	M	Number of Namespaces (NN)	0x00000001
521:520	M	Optional NVM Command Support (ONCS)	0x005D
523:522	M	Fused Operation Support (FUSES)	0x0000
524	M	Format NVM Attributes (FNA)	0x00
525	M	Volatile Write Cache (VWC)	0x01
527:526	M	Atomic Write Unit Normal (AWUN)	TBD
529:528	M	Atomic Write Unit Power Fail (AWUPF)	TBD
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Namespace Write Protection Capabilities (NWPC)	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0000
535:534	-	Reserved	0x0000
539:536	O	SGL Support (SGLS)	0x00000000
543:540	O	Maximum Number of Allowed Namespace, if supports ANA Reporting shall not be 0 and less than NN (MNAN)	0x00
767:544	-	Reserved	0x00
IO Command Set Attributes			
1023:768	M	NVM Subsystem NVMe Qualified Name (SUBNQN)	0x00
1791:1024	-	Reserved	0x00
2047:1792	-	Refer to the NVMe over Fabrics specification	0x00
2079:2048	M	Power State 0 Descriptor (PSD0)	0x00
2111:2080	O	Power State 1 Descriptor (PSD1)	0x00
2143:2112	O	Power State 2 Descriptor (PSD2)	0x00
2175:2144	O	Power State 3 Descriptor (PSD3)	0x00
2207:2176	O	Power State 4 Descriptor (PSD4)	0x00
2239:2208	O	Power State 5 Descriptor (PSD5)	0x00
2271:2240	O	Power State 6 Descriptor (PSD6)	0x00
2303:2272	O	Power State 7 Descriptor (PSD7)	0x00
Bytes	**O/M**	**Description**	**Default Value**
2335:2304	O	Power State 8 Descriptor (PSD8)	0x00
2367:2336	O	Power State 9 Descriptor (PSD9)	0x00

2399:2368	O	Power State 10 Descriptor (PSD10)	0x00
2431:2400	O	Power State 11 Descriptor (PSD11)	0x00
2463:2432	O	Power State 12 Descriptor (PSD12)	0x00
2495:2464	O	Power State 13 Descriptor (PSD13)	0x00
2527:2496	O	Power State 14 Descriptor (PSD14)	0x00
2559:2528	O	Power State 15 Descriptor (PSD15)	0x00
2591:2560	O	Power State 16 Descriptor (PSD16)	0x00
2623:2592	O	Power State 17 Descriptor (PSD17)	0x00
2655:2624	O	Power State 18 Descriptor (PSD18)	0x00
2687:2656	O	Power State 19 Descriptor (PSD19)	0x00
2719:2688	O	Power State 20 Descriptor (PSD20)	0x00
2751:2720	O	Power State 21 Descriptor (PSD21)	0x00
2783:2752	O	Power State 22 Descriptor (PSD22)	0x00
2815:2784	O	Power State 23 Descriptor (PSD23)	0x00
2847:2816	O	Power State 24 Descriptor (PSD24)	0x00
2879:2848	O	Power State 25 Descriptor (PSD25)	0x00
2911:2880	O	Power State26 Descriptor (PSD26)	0x00
2943:2912	O	Power State 27 Descriptor (PSD27)	0x00
2975:2944	O	Power State 28 Descriptor (PSD28)	0x00
3007:2976	O	Power State 29 Descriptor (PSD29)	0x00
3039:3008	O	Power State 30 Descriptor (PSD30)	0x00
3071:3040	O	Power State 31 Descriptor (PSD31)	0x00
Vendor Specific			
4095:3072	O	Vendor Specific (VS)	Vendor Reserved

***** The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at http://standards.ieee.org/develop/regauth/oui/public.html.

****** Depends on the using of capacity

Table 6-6 Identify Namespace Data Structure & NVM Command Set Specific

Bytes	O/M	Description	Default Value
7:0	M	Namespace Size (NSZE)	TBD*
15:8	M	Namespace Capacity (NCAP)	TBD*
23:16	M	Namespace Utilization (NUSE)	TBD*
24	M	Namespace Features (NSFEAT)	0x00
25	M	Number of LBA Formats (NLBAF)	0x01
26	M	Formatted LBA Size (FLBAS)	0x00
27	M	Metadata Capabilities (MC)	0x00
28	M	End-to-end Data Protection Capabilities (DPC)	0x00
29	M	End-to-end Data Protection Type Settings (DPS)	0x00
30	O	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)	0x00
31	O	Reservation Capabilities (RESCAP)	0x00
32	O	Format Progress Indicator (FPI)	0x00
33	O	Deallocate Logical Block Features (dlfeat)	0x09
35:34	O	Namespace Atomic Write Unit Normal (NAWUN)	0x0000
37:36	O	Namespace Atomic Write Unit Power Fail (NAWUPF)	0x0000
39:38	O	Namespace Atomic Compare & Write Unit (NACWU)	0x0000
41:40	O	Namespace Atomic Boundary Size Normal (NABSN)	0x0000
43:42	O	Namespace Atomic Boundary Offset (NABO)	0x0000
45:44	O	Namespace Atomic Boundary Size Power Fail (NABSPF)	0x0000
47:46	O	Namespace Optimal IO Boundary (NOIOB)	0x0000
63:48	O	NVM Capacity (NVMCAP)	0x00
65:64	O	Namespace Preferred Write Granularity (NPWG)	0x00
67:66	O	Namespace Preferred Write Alignment (NPWA)	0x00
69:68	O	Namespace Preferred Deallocation(Trim) Granularity (NPDG)	0x00
71:70	O	Namespace Preferred Deallocation(Trim) Alignment (NPDA)	0x00
73:72	O	Namespace Optimal Write Size (NOWS)	0x00
91:74	-	Reserved	0x00
95:92	O	ANA Groput Identifier (anagrpid)	0x00
Bytes	**O/M**	**Description**	**Default Value**

98:96	-	Reserved	0x00
99	O	Namespace Attributes (NSATTR)	0x00
101:100	O	NVM Set Identifier (nvmsetid)	0x00
103:102	O	Endurange Group Identifier // NVMe 1.4 add (endgid)	0x00
119:104	O	Namespace Globally Unique Identifier (NGUID)	0x00
127:120	O	IEEE Extended Unique Identifier (EUI64)	0x373900F0FFA77964
131:128	M	LBA Format 0 Support (LBAF0)	0x02090000
135:132	O	LBA Format 1 Support (LBAF1)	0x00000000
139:136	O	LBA Format 2 Support (LBAF2)	0x00000000
143:140	O	LBA Format 3 Support (LBAF3)	0x00000000
147:144	O	LBA Format 4 Support (LBAF4)	0x00000000
151:148	O	LBA Format 5 Support (LBAF5)	0x00000000
155:152	O	LBA Format 6 Support (LBAF6)	0x00000000
159:156	O	LBA Format 7 Support (LBAF7)	0x00000000
163:160	O	LBA Format 8 Support (LBAF8)	0x00000000
167:164	O	LBA Format 9 Support (LBAF9)	0x00000000
171:168	O	LBA Format 10 Support (LBAF10)	0x00000000
175:172	O	LBA Format 11 Support (LBAF11)	0x00000000
179:176	O	LBA Format 12 Support (LBAF12)	0x00000000
183:180	O	LBA Format 13 Support (LBAF13)	0x00000000
187:184	O	LBA Format 14 Support (LBAF14)	0x00000000
191:188	O	LBA Format 15 Support (LBAF15)	0x00000000
383:192	-	Reserved	0x00
4095:384	O	Vendor Specific (VS)	0x00

* See IDEMA SPEC

** See IEEE EUI-64 SPEC

■ List of Identify Namespace Data Structure for Each Capacity

Capacity (GB)	Byte[7:0]: Namespace Size (NSZE)
480	37E436B0h
960	6FC81AB0h
1920	DF8FE2B0h
3840	1BF1F72B0h
7680	37E3E92B0h

6.3. SMART Attributes

■ **SMART Attributes (Log Identifier 02h)**

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1 (CTRL Tj)
[203:202]	2	Temperature Sensor 2 (N/A)
[205:204]	2	Temperature Sensor 3 (N/A)
[207:206]	2	Temperature Sensor 4 (N/A)
[209:208]	2	Temperature Sensor 5 (N/A)
[211:210]	2	Temperature Sensor 6 (N/A)
[213:212]	2	Temperature Sensor 7 (N/A)
[215:214]	2	Temperature Sensor 8 (N/A)
[511:216]	296	Reserved

7. ACRONYMS

Acronym	Definition
AES	Advanced Encryption Standard
ATTO	Commercial performance benchmark application
DDR	Double Data Rate (SDRAM)
ASPM	Active States Power Management
APST	Autonomous Power State Transition
LBA	Logical Block Addressing
MTBF	Mean Time Between Failures
NVMe	Non-Volatile Memory Express
OPAL	Open Physics Abstraction Layer
PCBA	Printed Circuit Board Assembly
PCIe	PCI Express / Peripheral Component Interconnect Express
PSID	Physical Security ID
SMART	Self-Monitoring, Analysis and Reporting Technology
TLC	Tipple Level Cell

8. PART NUMBER DECODER

M2P80-AH$X^1X^2X^3X^4X^5X^6X^7X^8$

Item	Series	Capacity	NAND Flash & Temperature Grade	Option
		X^1 X^2 X^3 X^4 X^5	**X^6**	**X^7 X^8**
M2P80	**AH**	**0480G** (480GB) **0960G** (960GB) **1920G** (1920GB) **3840G** (3840GB) **7680G** (7960GB)	**A** : 3D TLC , Standard (0˚C to +70˚C) **B** : 3D TLC , Wide (-40˚C to +85˚C)	See below

X^7 X^8 (Reserved for specific requirement)

Blank: Standard