

**Amtron Technology, Inc.**

**Industrial Grade M.2 2280 PCIe SSD**

AC Series

Product Datasheet

V1.9

## Table of Contents

|   |           |
|---|-----------|
| <b>1. Introduction .....</b>                    | <b>4</b>  |
| 1.1. Description.....                           | 4         |
| 1.2. Product Features .....                     | 4         |
| 1.3. Product Overview .....                     | 5         |
| 1.4. Product Dimension .....                    | 6         |
| 1.5. Block Diagram.....                         | 8         |
| <b>2. Product Specifications.....</b>           | <b>9</b>  |
| 2.1. Specifications.....                        | 9         |
| 2.2. Device Capacity.....                       | 9         |
| 2.3. Performance .....                          | 10        |
| 2.4. POR/SPOR Standby Ready Time.....           | 11        |
| 2.5. Thermal Throttling.....                    | 12        |
| 2.6. TCG Opal 2.0.....                          | 14        |
| 2.7. TBW (Terabytes Written).....               | 15        |
| 2.8. UBER (Uncorrectable Bit Error Rates) ..... | 15        |
| 2.9. MTBF .....                                 | 16        |
| <b>3. Environmental Specifications .....</b>    | <b>17</b> |
| 3.1. Environmental Conditions .....             | 17        |
| 3.1.1. Temperature and Humidity .....           | 17        |
| 3.1.2. Shock .....                              | 18        |
| 3.1.3. Vibration .....                          | 18        |
| 3.1.4. Drop .....                               | 18        |
| 3.1.5. Bending.....                             | 18        |
| 3.1.6. Electrostatic Discharge (ESD).....       | 18        |
| 3.1.7. EMI Compliance.....                      | 18        |
| 3.2. Certification & Compliance.....            | 18        |
| <b>4. Electrical Specifications .....</b>       | <b>19</b> |
| 4.1. Supply Voltage .....                       | 19        |
| 4.2. Power Consumption.....                     | 19        |
| <b>5. Interface.....</b>                        | <b>20</b> |

5.1. Pin Assignment and Descriptions ..... 20

**6. Supported Commands ..... 23**

6.1. NVMe Command List ..... 23

6.2. Identify Device Data ..... 25

6.3. SMART Attributes ..... 31

**7. ACRONYMS ..... 32**

**8. Part Number Decoder ..... 33**

## 1. INTRODUCTION

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### 1.1. Description

Amtron industrial AC series M.2 2280 PCIe SSD is designed with PCIe Gen3 x4 interface and is fully compliant with the standard Next Generation Form Factor (NGFF). It can reach up to 3300 MB/s read and 1000 MB/s write high performance. These M.2 PCIe modules are offered in standard temperature grade (0°C to +70°C) and wide temperature grade (-40°C to +85°C). The memory capacities are available from 240GB to 1920GB.

### 1.2. Product Features

- M.2 2280-M form factor
- PCI Express Base Version 3.1 and Compliant with NVMe 1.3d
- PCIe Gen3 x 4 lane & backward compatible to PCIe Gen2 and Gen1
- RoHS compliant [Lead free]
- 3D Triple Level Cell (TLC) NAND Flash
- Capacity from 240GB up to 1920GB
- High speed:  
Read 3,300 MB/s max., Write 3,000 MB/s max.
- Endure severe thermal and dynamic environments
- Very low power consumption
- MTBF > 2,000,000 hours \*
- Support SMART and TRIM Command
- Controlled Bill of Materials (BOM )

**\*Note:** Lower MTBF is expected for higher capacity drives. To be conservative, the lowest MTBF is reported in this document

### 1.3. Product Overview

- **Form Factor**
  - M.2 2280-M
- **PCIe Interface**
  - NVMe PCIe Gen3 x4
  - NVMe 1.3d
  - PCI Express Base 3.1
- **Capacity**
  - 240GB up to 1920GB
- **Flash Interface**
  - Flash Type: 3D TLC BGA
  - Up to 4 pcs of BGA152 flash
- **Performance**
  - Read up to 3,300 MB/s
  - Write up to 1,000 MB/s
- **Reliability**
  - MTBF <sup>1</sup> > 2,000,000 hours
  - Uncorrectable Bit Error Rate (UBER)  
< 1 sector per 10<sup>16</sup> bits read
- **Power Consumption** <sup>2</sup>
  - Active mode: < 6,000 mW
  - Idle mode: < 2,000 mW
- **ECC**
  - LDPC / RAID ECC
  - Low density parity check code  
( >120bit/Kbytes)
- **Compliant**
  - RoHS
- **Advanced Flash Management**
  - Advanced Wear Leveling
  - Bad Block Management
  - TRIM
  - SMART
  - Over-Provision
- **Temperature Range**
  - Operation (standard): 0°C to 70°C
  - Operation (wide): -40°C to 85° C
  - Storage: -40°C to 85°C
- **Features Support List**
  - TCG Pyrite/OPAL <sup>3</sup> (optional)
  - Thermal throttling
  - SmartECC™
  - SmartRefresh™
  - Write Protect
  - Secure Erase
  - Power Loss Protection (optional)
- **Safety Certification**
  - ISO 9001
  - ISO 14001
  - ISO 45001
  - ISO 27001
- **EMI Compliant**
  - EN55032, CISPR 32 (CE)
  - AS/NZS CISPR 32 (CE)
  - ANSI C63.4 (FCC)
  - CNS 13438 (BSMI)
  - VCCI-CISPR 32 (VCCI)

#### Note:

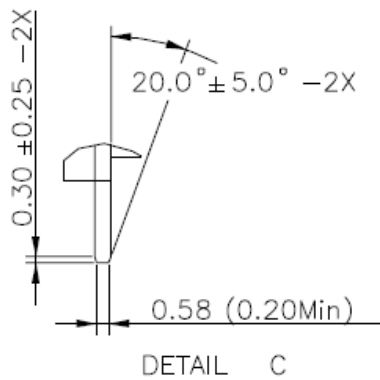
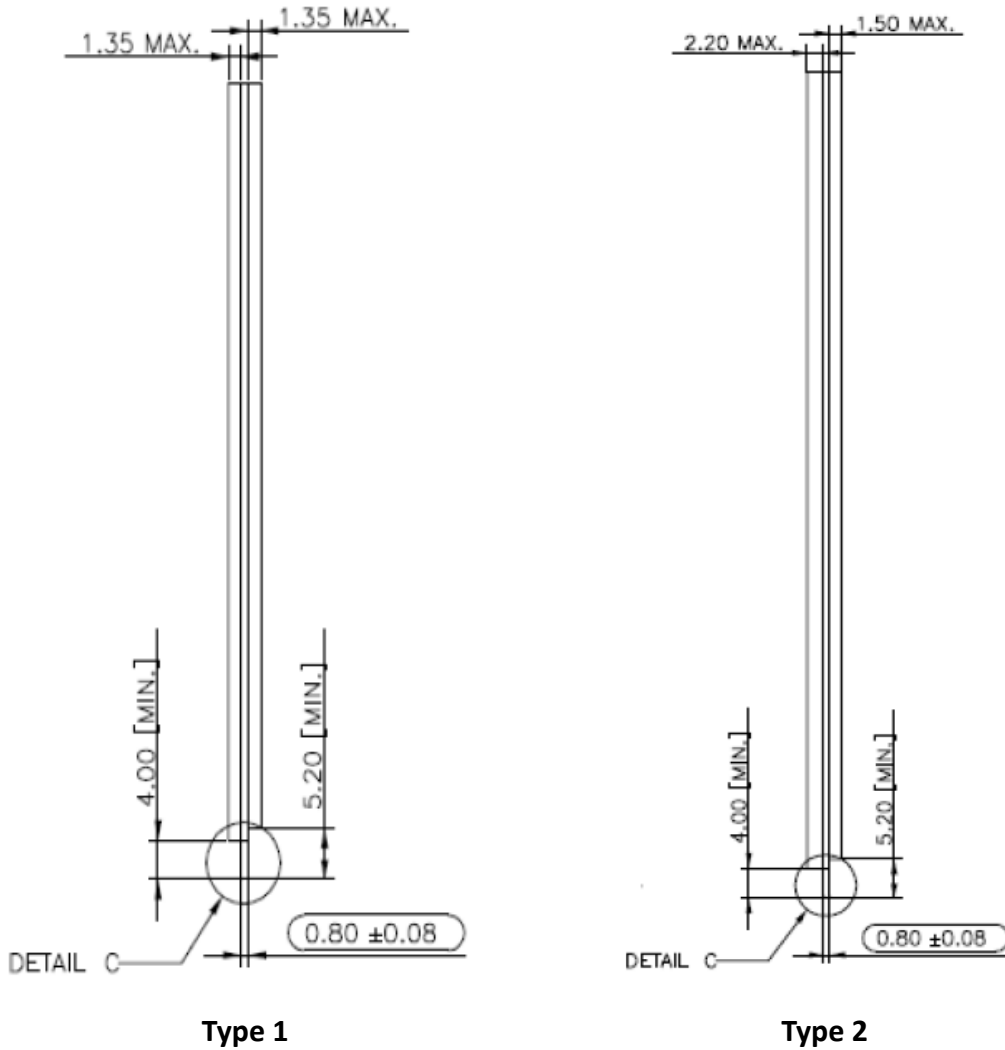
1. **MTBF** (mean time between failures) is a measure of how reliable a hardware product is..
2. See Section 4.2 “Power Consumption” for details.
3. OPAL + AES is supported by different production settings and firmware version

1.4. Product Dimension

Type1: Dimension: 80mm(L) x 22mm(W) x 3.5mm(H) for Non-PLP PCBA

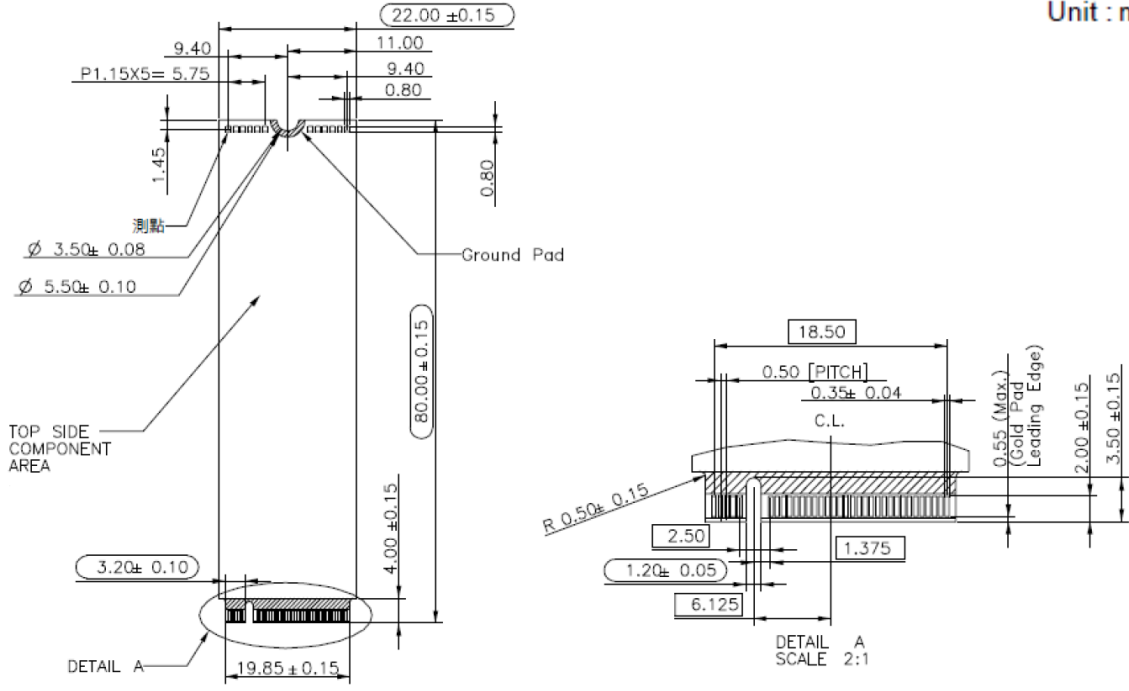
Type2: Dimension: 80mm(L) x 22mm(W) x 4.5mm(H) for PLP PCBA

Side View

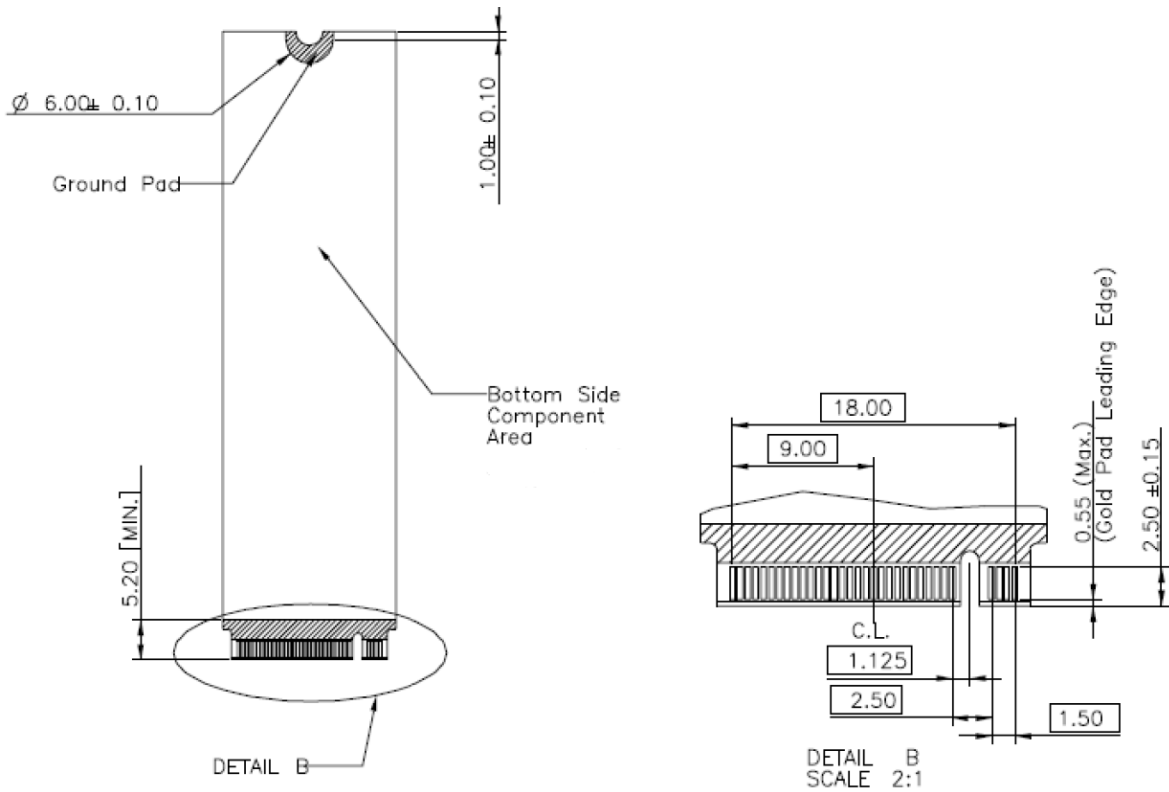


Top View

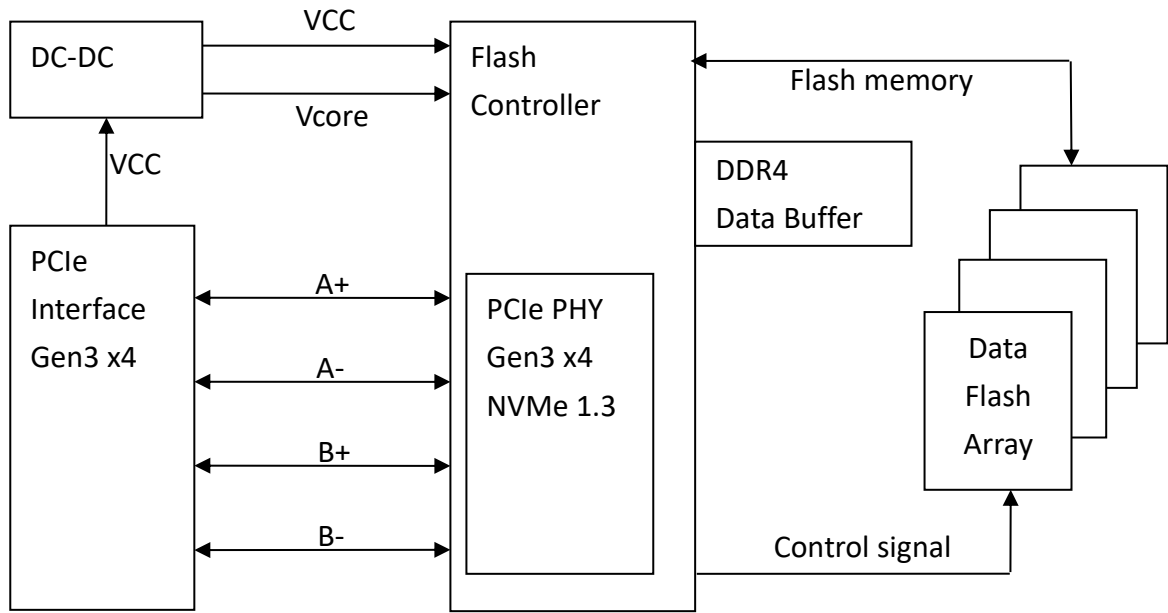
Unit : mm



Bottom View



1.5. Block Diagram



M.2 2280 PCIe SSD Block Diagram



## 2. PRODUCT SPECIFICATIONS



### 2.1. Specifications

- **Capacity**
  - 240GB up to 1920GB
- **Electrical/Physical Interface**
  - PCI Express Base Version 3.1
  - Compliant with NVMe 1.3d
  - PCIe Gen3 x 4 lane & backward compatible to PCIe Gen2 and Gen1
- **Support Hardware Power Loss Protection (Optional Feature)**
  - Protect data loss, even the last data, during write process when power sudden off.
  - Add-on Polymer Tantalum Capacitors hold-up several milliseconds to keep DRAM data write to NAND Flash.

### 2.2. Device Capacity

| Capacity | IDEMA Standard      |                     | User Data Size              |
|----------|---------------------|---------------------|-----------------------------|
|          | 512Bytes/Sector     | 4KBytes/Sector      |                             |
|          | Total Sectors (LBA) | Total Sectors (LBA) |                             |
| 240GB    | 468,862,128         | 58,607,766          | Depended on file management |
| 480GB    | 937,703,088         | 117,212,886         |                             |
| 960GB    | 1,875,385,008       | 234,423,126         |                             |
| 1920GB   | 3,750,748,848       | 468,843,606         |                             |

**Notes:**

1. 1 Gigabyte (GB) is equal to 1,000,000,000 Bytes; 1 sector is equal to 512 Bytes.
2. The calculation is following IDEMA Standard.
3. The total actual user data size of the SSD may be less than device capacity due to SSD format, SSD partition, operating system.  
EX: OS shows 223.57GB (NTFS) with 240GB SSD.

## 2.3. Performance

- Sequential Read/Write Performance

| Capacity | Flash Structure          | Sequential  |              | 4K Random   |              |
|----------|--------------------------|-------------|--------------|-------------|--------------|
|          |                          | Read (MB/s) | Write (MB/s) | Read (IOPS) | Write (IOPS) |
| 240GB    | 64GB x4, BGA BiCS3, DDP  | 2,800       | 340          | 101K        | 13K          |
| 480GB    | 128GB x4, BGA BiCS3, QDP | 3,000       | 580          | 170K        | 18K          |
| 960GB    | 256GB x4, BGA BiCS3, ODP | 2,600       | 1,000        | 200K        | 20K          |
| 1920GB   | 512GB x4, BGA BiCS3, ODP | 2,500       | 900          | 200K        | 20K          |
| 240GB    | 64GB x4, BGA BiCS4, DDP  | 3,300       | 360          | 110K        | 11K          |
| 480GB    | 128GB x4, BGA BiCS4, QDP | 3,300       | 580          | 200K        | 15K          |
| 960GB    | 256GB x4, BGA BiCS4, ODP | 3,300       | 1,000        | 200K        | 24K          |
| 1920GB   | 512GB x4, BGA BiCS4, ODP | 3,300       | 1,000        | 200K        | 24K          |
| 240GB    | 128GB x2, BGA BiCS5, DDP | 1,400       | 160          | 50K         | 35K          |
| 480GB    | 128GB x4, BGA BiCS5, DDP | 3,300       | 350          | 100K        | 80K          |
| 960GB    | 256GB x4, BGA BiCS5, QDP | 3,300       | 750          | 200K        | 160K         |
| 1920GB   | 512GB x4, BGA BiCS5, ODP | 3,300       | 1,000        | 200K        | 200K         |

**Notes:**

1. Performance may differ according to flash configuration and platform.
2. Performance specification is under Thermal Throttling inactivated.
3. The data shows the sustained and average performance.
4. Performance is measured with the follow conditions
  1. CrystalDiskMark 6.0, 1GB range, QD32T1 for sequential
  2. FIO on Linux version with QD32 for IOPS
  3. OS: Win10 64bit was, version 1709
  4. Intel Core i7-8700K CPU @ 3.70GHz
5. Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH, DC+3.3V condition.

## 2.4. POR/SPOR Standby Ready Time

- **POR/SPOR Ready Time**

| Capacity | POR ready time |      | SPOR ready time |       |
|----------|----------------|------|-----------------|-------|
|          | Typ.           | Max. | Typ.            | Max.  |
| 240GB    | 120            | 150  | 2,000           | 8,000 |
| 480GB    | 120            | 150  | 3,000           | 8,000 |
| 960GB    | 120            | 150  | 3,500           | 8,000 |
| 1920GB   | 120            | 150  | 3,500           | 8,000 |

Unit: ms

**Notes:**

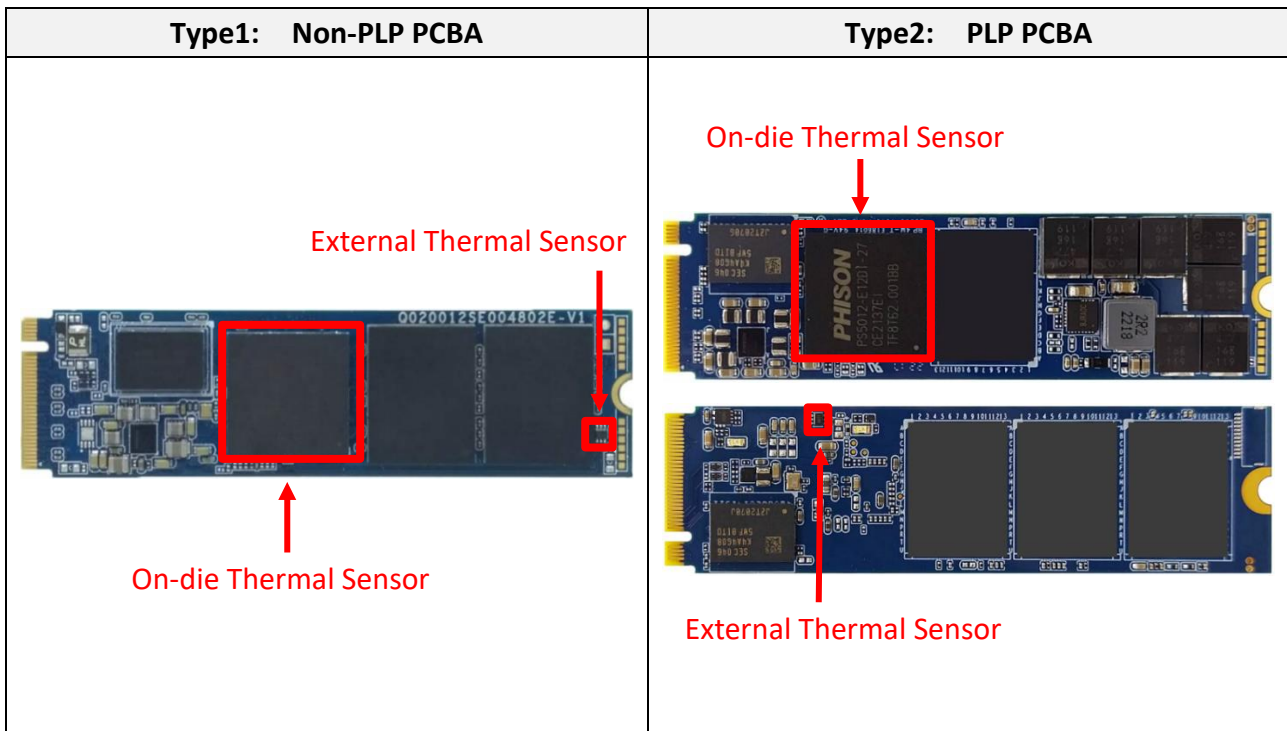
1. POR/SPOR stands for following:
  - (a.) POR: Power On Ready. (The ready time variation depends on data recover size.)
  - (b.) SPOR: Power On Ready after Sudden Power Off. (The ready time variation depends on data recover size.)
2. POR/SPOR ready time stands for following:
 

Power on Time: From Power On to SSD response after drive ready.
3. Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH, DC+3.3V condition.

## 2.5. Thermal Throttling

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. The controller is designed with an on-die thermal sensor and with its accuracy, firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via S.M.A.R.T. reading.

- **Purpose of Thermal Throttling:**
  - In order to keep the optimal performance in the safe range of the temperature.
- **Thermal sensors:**
  - We have external thermal sensor & on-die thermal sensor (internal controller) to detect temperature. There is 1pcs external thermal sensor on PCB, the position depends on different form factor (The thermal sensor is shown below. The picture is for reference only).
  - External thermal sensor would detect flash temperature; On-die thermal sensor detect controller temperature.



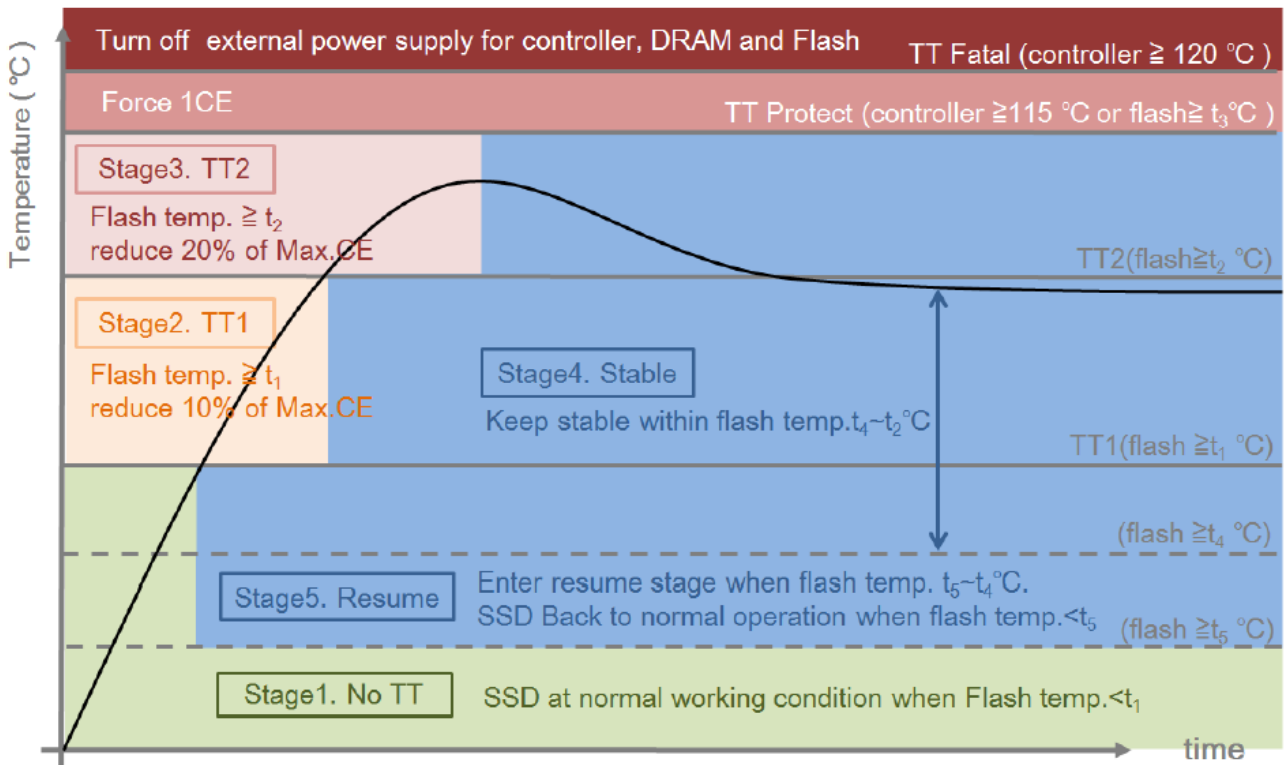


Figure 2-1 Thermal Throttling Schematic

|                      | Operation temp. of Normal-temp. grade: 0-70°C | Operation temp. of Wide-temp. grade: -40-85°C |
|----------------------|---|---|
| <b>t<sub>1</sub></b> | 68°C  | 82°C  |
| <b>t<sub>2</sub></b> | 70°C  | 85°C  |
| <b>t<sub>3</sub></b> | 80°C  | 95°C  |
| <b>t<sub>4</sub></b> | 64°C  | 78°C  |
| <b>t<sub>5</sub></b> | 60°C  | 74°C  |

**Notes:**

1. TT shown on Figure 2-1 means “Thermal Throttling”.
2. CE = Chip Enable.
3. temp. = temperature

## 2.6. TCG Opal 2.0

The Opal specification is a set of specifications for self-encrypting drives published by the Trusted Computing Group (TCG), a non-profit organization that develops, defines, and promotes standards and specifications for secure computing. The Opal Security Subsystem Class(SSC) 2.0 defines the details of data management in storage devices and the classes authority for data access, and secures data from theft and tampering by unauthorized persons who are able to gain access to the storage device or host system.

### TCG Opal 2.0 Main Features:

- AES 256-bit Hardware Self Encryption
- Deploy Storage Device & Take Ownership:  
The Storage Device is integrated into its target system and ownership transferred by setting or changing the Storage Device's owner credential.
- Activate or Enroll Storage Device:  
LBA ranges are configured and data encryption and access control credentials (re)generated and/or set on the Storage Device. Access control is configured for LBA range unlocking.
- Lock & Unlock Storage Device:  
Unlocking of one or more LBA ranges by the host and locking of those ranges under host control via either an explicit lock or implicit lock triggered by a reset event. MBR shadowing provides a mechanism to boot into a secure pre-boot authentication environment to handle device unlocking.
- Repurpose & End-of-Life:  
Erasure of data within one or more.
- Physical Presence SID (PSID):  
PSID is defined by TCG OPAL as a 32-character string and the purpose is to revert SSD back to its manufacturing setting when the drive is still OPAL-activated. PSID code can be printed on a SSD label when an OPAL-activated SSD supports PSID revert feature.

## 2.7. TBW (Terabytes Written)

| Capacity | Flash Type               | TBW   | DWPD |
|----------|--------------------------|-------|------|
| 240GB    | 64GB x4, BGA BiCS3, DDP  | 390   | 0.8  |
| 480GB    | 128GB x4, BGA BiCS3, QDP | 800   | 0.8  |
| 960GB    | 256GB x4, BGA BiCS3, ODP | 1,580 | 0.8  |
| 1920GB   | 512GB x4, BGA BiCS3, ODP | 3,150 | 0.8  |
| 240GB    | 64GB x4, BGA BiCS4, DDP  | 270   | 0.6  |
| 480GB    | 128GB x4, BGA BiCS4, QDP | 580   | 0.7  |
| 960GB    | 256GB x4, BGA BiCS4, QDP | 1,180 | 0.7  |
| 1920GB   | 512GB x4, BGA BiCS4, ODP | 2,490 | 0.7  |
| 240GB    | 128GB x2, BGA BiCS5, DDP | 285   | 0.7  |
| 480GB    | 128GB x4, BGA BiCS5, DDP | 635   | 0.8  |
| 960GB    | 256GB x4, BGA BiCS5, QDP | 1,400 | 0.8  |
| 1920GB   | 512GB x4, BGA BiCS5, ODP | 2,800 | 0.8  |

### Notes:

1. TBW is measured by JEDEC Client 219A workload and calculated with PE count = 3000.
2. TBW may differ according to flash configuration and platform.
3. DWPD is calculated based on 5-year lifetime.
4. The SSD supports trim function. If Operation System does not support trim command, performance and TBW will be affected. (Like certain Windows OS, Linux kernel version before 2.6.33, other OS please reference each own user manual)
5. The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor.

## 2.8. UBER (Uncorrectable Bit Error Rates)

| Capacity | UBER                                      |
|----------|---|
| 240GB    | < 1 sector per 10 <sup>16</sup> bits read |
| 480GB    |   |
| 960GB    |   |
| 1920GB   |   |

### Notes:

1. UBER (Uncorrectable Bit Error Rates) means the uncorrectable error per bits read.
2. UBER = FER (fail rate) / Data Size (user data bit).

3. FER = uncorrectable ECC frame number / total ECC frame number.
4. The LDPC for TLC ECC capability > 120bit/KB.

## 2.9. MTBF

**MTBF** (mean time between failures) is a measure of how reliable a hardware product is. Its value represents the average time between a failure repair and the next failure. The unit of MTBF is typically in hours. The higher the MTBF value, the higher the reliability of the product. Please note that a lower MTBF is expected for higher capacity drives. To be conservative, the lowest MTBF is reported in this document. The MTBF calculated in this document is based on a software tool, Relex 7.3 . The predicted MTBF for Amtron AC series M.2 PCIe SSD is >2,000,000 hours



### 3. ENVIRONMENTAL SPECIFICATIONS



#### 3.1. Environmental Conditions

##### 3.1.1. Temperature and Humidity

|                        | Mode                 | Min. | Max. | Unit |
|------------------------|----------------------|------|------|------|
| Temperature Ranges     | Operation (Standard) | 0    | 70   | °C   |
|                        | Operation (Wide)     | -40  | 85   | °C   |
|                        | Storage              | -40  | 85   | °C   |
| Humidity               | Operation            | 5    | 95   | %    |
|                        | Storage              | 5    | 95   | %    |
| Temperature Cycle Test | Operation (Standard) | 0    | 70   | °C   |
|                        | Operation (Wide)     | -40  | 85   | °C   |
|                        | Storage              | -40  | 85   | °C   |

**Notes:**

1. The operation temperature means the case temperature, in which can be detected via the S.M.A.R.T. Airflow is suggested and it will allow device to be operated at appropriate temperature for each component during heavy workloads environment.

3.1.2. Shock

■ Shock Specification

|                 | Acceleration Force |
|-----------------|--------------------|
| Non-Operational | 1500G              |
| Operational     | 1500G              |

3.1.3. Vibration

■ Vibration Specification

|                 | Condition              |                        |
|-----------------|------------------------|------------------------|
|                 | Frequency/Displacement | Frequency/Acceleration |
| Non-Operational | 20Hz~80Hz/1.52mm       | 80Hz~2000Hz/20G        |

3.1.4. Drop

■ Drop Specification

|                 | Height of Drop | Number of Drop      |
|-----------------|----------------|---------------------|
| Non-operational | 80cm free fall | 6 face of each unit |

3.1.5. Bending

■ Bending Specification

|                 | Force | Action           |
|-----------------|-------|------------------|
| Non-operational | ≥ 20N | Hold 1min/5times |

3.1.6. Electrostatic Discharge (ESD)

| Specification  | +/- 4KV   |
|--|---|
| EN 55024, CISPR 24<br>EN 61000-4-2 and IEC 61000-4-2 | Device functions are affected, but EUT will be back to its normal or operational state automatically. |

3.1.7. EMI Compliance

| Specification   |
|---|
| EN 55032, CISPR 32 (CE)<br>AS/NZS CISPR 32 (CE)<br>ANSI C63.4 (FCC)<br>VCCI-CISPR 32 (VCCI)<br>CNS 13438 (BSMI) |

3.2. Certification & Compliance

- RoHS

## 4. ELECTRICAL SPECIFICATIONS



### 4.1. Supply Voltage

| Parameter                      | Rating        |
|--------------------------------|---------------|
| Operating Voltage              | 3.3V ± 5%     |
| Rise Time (Max/Min)            | 100ms / 0.1ms |
| Fall Time (Max/Min)            | 5s / 1ms      |
| Min. off Time <sup>Note1</sup> | 1s            |

**Notes:**

1. Minimum time between power removed from SSD (Vcc < 100 mV) and power re-applied to the drive.
2. Ensure the voltage of each power domain in SSD has enough time to discharge less than 0.1V.
3. Rise Time during from 10% to 90% of 3.3V.
4. Fall Time during from 90% to 10% of 3.3V.

### 4.2. Power Consumption

| Capacity | Flash Type               | Read  | Write | Idle  |
|----------|--------------------------|-------|-------|-------|
| 240GB    | 64GB x4, BGA BiCS3, DDP  | 3,900 | 2,700 | 2,000 |
| 480GB    | 128GB x4, BGA BiCS3, QDP | 4,100 | 3,400 | 2,000 |
| 960GB    | 256GB x4, BGA BiCS3, ODP | 5,000 | 5,300 | 2,000 |
| 1920GB   | 512GB x4, BGA BiCS3, ODP | 5,200 | 5,000 | 2,000 |
| 240GB    | 64GB x4, BGA BiCS4, DDP  | 4,500 | 3,500 | 2,000 |
| 480GB    | 128GB x4, BGA BiCS4, QDP | 4,800 | 4,500 | 2,000 |
| 960GB    | 256GB x4, BGA BiCS4, QDP | 5,000 | 5,000 | 2,000 |
| 1920GB   | 512GB x4, BGA BiCS4, ODP | 5,200 | 5,800 | 2,000 |
| 240GB    | 128GB x2, BGA BiCS5, DDP | 4,000 | 3,300 | 2,000 |
| 480GB    | 128GB x4, BGA BiCS5, DDP | 5,000 | 4,800 | 2,000 |
| 960GB    | 256GB x4, BGA BiCS5, QDP | 5,200 | 5,800 | 2,000 |
| 1920GB   | 512GB x4, BGA BiCS5, ODP | 5,500 | 6,000 | 2,000 |

Unit: mW

**Notes:**

1. Use CrystalDiskMark 6.0 with the setting of 1000MB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5].
2. Power Consumption may differ according to flash configuration and platform.
3. The measured power voltage is 3.3V.
4. Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH.

## 5. INTERFACE



### 5.1. Pin Assignment and Descriptions

The follow table defines the signal assignment of the internal NGFF connector for SSD usage, described in the PCI Express M.2 Specification version 1.1 of the PCI-SIG.



| Pin # | SATA Pin | Description  |
|-------|----------|--|
| 1     | GND      | Ground   |
| 2     | 3.3V     | 3.3V source  |
| 3     | GND      | Ground   |
| 4     | 3.3V     | 3.3V source  |
| 5     | PETn3    | PCIe TX Differential signal defined by the PCI Express M.2 spec  |
| 6     | N/C      | No connect   |
| 7     | PETp3    | PCIe TX Differential signal defined by the PCI Express M.2 spec  |
| 8     | N/C      | No connect   |
| 9     | GND      | Ground   |
| 10    | LED1#    | Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system. |
| 11    | PERn3    | PCIe RX Differential signal defined by the PCI Express M.2 spec  |
| 12    | 3.3V     | 3.3V source  |
| 13    | PERp3    | PCIe RX Differential signal defined by the PCI Express M.2 spec  |
| 14    | 3.3V     | 3.3V source  |
| 15    | GND      | Ground   |
| 16    | 3.3V     | 3.3V source  |
| 17    | PETn2    | PCIe RX Differential signal defined by the PCI Express M.2 spec  |
| 18    | 3.3V     | 3.3V source  |
| 19    | PETp2    | PCIe RX Differential signal defined by the PCI Express M.2 spec  |
| 20    | N/C      | No connect   |
| 21    | GND      | Ground   |
| 22    | N/C      | No connect   |
| 23    | PERn2    | PCIe RX Differential signal defined by the PCI Express M.2 spec  |
|       |          |  |

| Pin # | SATA Pin               | Description   |
|-------|------------------------|---|
| 24    | N/C                    | No connect  |
| 25    | PERp2                  | PCIe RX Differential signal defined by the PCI Express M.2 spec   |
| 26    | N/C                    | No connect  |
| 27    | GND                    | Ground  |
| 28    | N/C                    | No connect  |
| 29    | PETn1                  | PCIe TX Differential signal defined by the PCI Express M.2 spec   |
| 30    | N/C                    | No connect  |
| 31    | PETp1                  | PCIe TX Differential signal defined by the PCI Express M.2 spec   |
| 32    | N/C                    | No connect  |
| 33    | GND                    | Ground  |
| 34    | N/C                    | No connect  |
| 35    | PERn1                  | PCIe RX Differential signal defined by the PCI Express M.2 spec   |
| 36    | N/C                    | No connect  |
| 37    | PERp1                  | PCIe RX Differential signal defined by the PCI Express M.2 spec   |
| 38    | N/C                    | No connect  |
| 39    | GND                    | Ground  |
| 40    | SMB_CLK (I/O)(0/1.8V)  | SMBus Clock; Open Drain with pull-up on platform.   |
| 41    | PETn0                  | PCIe TX Differential signal defined by the PCI Express M.2 spec   |
| 42    | SMB_DATA (I/O)(0/1.8V) | SMBus Data; Open Drain with pull-up on platform.  |
| 43    | PETp0                  | PCIe TX Differential signal defined by the PCI Express M.2 spec   |
| 44    | ALERT#(O)(0/1.8V)      | -   |
| 45    | GND                    | Ground  |
| 46    | N/C                    | No connect  |
| 47    | PERn0                  | PCIe RX Differential signal defined by the PCI Express M.2 spec   |
| 48    | N/C                    | No connect  |
| 49    | PERp0                  | PCIe RX Differential signal defined by the PCI Express M.2 spec   |
| 50    | PERST#(I)(0/3.3V)      | PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.                                       |
| 51    | GND                    | Ground  |
| 52    | CLKREQ#(I/O)(0/3.3V)   | Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states. |
| 53    | REFCLKn                | PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.   |
| 54    | PEWAKE#(I/O)(0/3.3V)   | -   |
| 55    | REFCLKp                | PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.   |
|       |                        |   |

| Pin # | SATA Pin                     | Description  |
|-------|------------------------------|--|
| 56    | Reserved for MFG DATA        | Manufacturing Data line. Used for SSD manufacturing only.<br>Not used in normal operation.<br>Pins should be left N/C in platform Socket.  |
| 57    | GND                          | Ground   |
| 58    | Reserved for MFG CLOCK       | Manufacturing Clock line. Used for SSD manufacturing only.<br>Not used in normal operation.<br>Pins should be left N/C in platform Socket. |
| 59    | Module Key M                 | Module Key   |
| 60    | Module Key M                 |  |
| 61    | Module Key M                 |  |
| 62    | Module Key M                 |  |
| 63    | Module Key M                 |  |
| 64    | Module Key M                 |  |
| 65    | Module Key M                 |  |
| 66    | Module Key M                 |  |
| 67    | N/C                          | No Connect   |
| 68    | SUSCLK(32KHz)<br>(I)(0/3.3V) | -  |
| 69    | N/C                          | PEDET (NC-PCIe).<br>No Connect for PCIe.   |
| 70    | 3.3V                         | 3.3V source  |
| 71    | GND                          | Ground   |
| 72    | 3.3V                         | 3.3V source  |
| 73    | GND                          | Ground   |
| 74    | 3.3V                         | 3.3V source  |
| 75    | GND                          | Ground   |

## 6. SUPPORTED COMMANDS



### 6.1. NVMe Command List

**Table 6-1 Admin Commands**

| Op-Code | O/M | Command Description         |
|---------|-----|-----------------------------|
| 00h     | M   | Delete I/O Submission Queue |
| 01h     | M   | Create I/O Submission Queue |
| 02h     | M   | Get Log Page                |
| 04h     | M   | Delete I/O Completion Queue |
| 05h     | M   | Create I/O Completion Queue |
| 06h     | M   | Identify                    |
| 08h     | M   | Abort                       |
| 09h     | M   | Set Features                |
| 0Ah     | M   | Get Features                |
| 0Ch     | M   | Asynchronous Event Request  |
| 10h     | O   | Firmware Activate           |
| 11h     | O   | Firmware Image Download     |
| 14h     | O   | Device Self-test            |
| 80h     | O   | Format NVM                  |
| 81h     | O   | Security Send               |
| 82h     | O   | Security Receive            |
| 84h     | O   | Sanitize                    |

**Table 6-2 I/O Commands**

| Op-Code | O/M | Command Description |
|---------|-----|---------------------|
| 00h     | O   | Flush               |
| 01h     | O   | Write               |
| 02h     | O   | Read                |
| 04h     | O   | Write Uncorrectable |
| 05h     | O   | Compare             |
| 08h     | O   | Write Zeroes        |
| 09h     | O   | Dataset Management  |

**Table 6-3 Set Feature Commands**

| Op-Code   | O/M | Command Description                |
|-----------|-----|------------------------------------|
| 00h       |     | Reserved                           |
| 01h       | M   | Arbitration                        |
| 02h       | M   | Power Management                   |
| 03h       | O   | LBA Range Type                     |
| 04h       | M   | Temperature Threshold              |
| 05h       | M   | Error Recovery                     |
| 06h       | O   | Volatile Write Cache               |
| 07h       | M   | Number of Queues                   |
| 08h       | M   | Interrupt Coalescing               |
| 09h       | M   | Interrupt Vector Configuration     |
| 0Ah       | M   | Write Atomicity Normal             |
| 0Bh       | M   | Asynchronous Event Configuration   |
| 0Ch       | O   | Autonomous Power State Transition  |
| 0Dh       | O   | Host Memory Buffer                 |
| 0Eh       | O   | Timestamp                          |
| 10h       | O   | Host Controlled Thermal Management |
| 11h       | O   | Non-Operational Power State Config |
| 0Eh – 7Dh |     | Reserved                           |
| 80h       | O   | Software Progress Marker           |

**Table 6-4 Get Log Page Commands**

| Op-Code   | O/M | Command Description        |
|-----------|-----|----------------------------|
| 00h       |     | Reserved                   |
| 01h       | M   | Error Information          |
| 02h       | M   | SMART / Health Information |
| 03h       | M   | Firmware Slot Information  |
| 04h       | O   | Changed Namespace List     |
| 06h       | O   | Device Self-test           |
| 09h – 7Fh |     | Reserved                   |
| 81h       | O   | Sanitize Status            |
| 82h - FFh |     | Reserved                   |



## 6.2. Identify Device Data

The following table details the sector data returned by the IDENTIFY DEVICE command.

### ■ Identify Controller Data Structure

| Bytes   | O/M | Default Value     | Description   |
|---------|-----|-------------------|---|
| 01:00   | M   | 0x1987            | PCI Vendor ID (VID)   |
| 03:02   | M   | 0x1987            | PCI Subsystem Vendor ID (SSVID)                                     |
| 23:04   | M   | TBD               | Serial Number (SN)  |
| 63:24   | M   | TBD               | Model Number (MN)   |
| 71:64   | M   | TBD               | Firmware Revision (FR)  |
| 72      | M   | 0x01              | Recommended Arbitration Burst (RAB)                                 |
| 75:73   | M   | 0x6479A7          | IEEE OUI Identifier (IEEE)  |
| 76      | O   | 0x00              | Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC) |
| 77      | M   | 0x09              | Maximum Data Transfer Size (MDTS)                                   |
| 79:78   | M   | 0x0001            | Controller ID (CNTLID)  |
| 83:80   | M   | 0x00010300        | Version (VER)   |
| 87:84   | M   | 0x00989680(10sec) | RTD3 Resume Latency (RTD3R)   |
| 91:88   | M   | 0x00989680(10sec) | RTD3 Entry Latency (RTD3E)  |
| 95:92   | M   | 0x00000200        | Optional Asynchronous Events Supported (OAES)                       |
| 99:96   | M   | 0x0002            | Controller Attributes (CTRATT)                                      |
| 111:100 | O   | 0x00              | Reserved  |
| 127:112 | O   | 0x00              | FRU Globally Unique Identifier (FGUID)                              |
| 239:128 | -   | 0x00              | Reserved  |
| 255:240 | -   | 0x00              | Refer to the NVMe Management Interface Specification for definition |
| 257:256 | M   | 0x0017            | Optional Admin Command Support (OACS)                               |
| 258     | M   | 0x03              | Abort Command Limit (ACL)   |
| 259     | M   | 0x03              | Asynchronous Event Request Limit (AERL)                             |
| 260     | M   | 0x12              | Firmware Updates (FRMW)   |
| 261     | M   | 0x08              | Log Page Attributes (LPA)   |
| 262     | M   | 0x3E              | Error Log Page Entries (ELPE)                                       |
| 263     | M   | 0x00              | Number of Power States Support (NPSS)                               |
| 264     | M   | 0x01              | Admin Vendor Specific Command Configuration (AVSCC)                 |
| 265     | O   | 0x00              | Autonomous Power State Transition Attributes (APSTA)                |
| 267:266 | M   | 0x016B            | Warning Composite Temperature Threshold (WCTEMP)                    |
| 269:268 | M   | 0x0170            | Critical Composite Temperature Threshold (CCTEMP)                   |
| 271:270 | O   | 0x64 10sec        | Maximum Time for Firmware Activation (MTFA)                         |

| Bytes                             | O/M | Default Value | Description   |
|-----------------------------------|-----|---------------|---|
| 275:272                           | O   | 0x00000000    | Host Memory Buffer Preferred Size (HMPRE)             |
| 279:276                           | O   | 0x00000000    | Host Memory Buffer Minimum Size (HMMIN)               |
| 295:280                           | O   | **            | Total NVM Capacity (TNVMCAP)                          |
| 311:296                           | O   | **            | Unallocated NVM Capacity (UNVMCAP)                    |
| 315:312                           | O   | 0x00000000    | Replay Protected Memory Block Support (RPMBS)         |
| 317:316                           | O   | 0x0A          | Extended Device Self-test Time (EDSTT)                |
| 318                               | O   | 0x00          | Device Self-test Options (DSTO)                       |
| 319                               | M   | 0x01          | Firmware Update Granularity (FWUG)                    |
| 321:320                           | M   | 0x0000        | Keep Alive Support (KAS)                              |
| 323:322                           | O   | 0x01          | Host Controlled Thermal Management Attributes (HCTMA) |
| 325:324                           | O   | 0x0139        | Minimum Thermal Management Temperature (MNTMT)        |
| 327:326                           | O   | 0x0166        | Maximum Thermal Management Temperature (MXTMT)        |
| 331:328                           | O   | 0x00000000    | Sanitize Capabilities (SANICAP)                       |
| 511:332                           | -   | 0x00          | Reserved  |
| <b>NVM Command Set Attributes</b> |     |               |   |
| 512                               | M   | 0x66          | Submission Queue Entry Size (SQES)                    |
| 513                               | M   | 0x44          | Completion Queue Entry Size (CQES)                    |
| 515:514                           | M   | 0x0100        | Maximum Outstanding Commands (MAXCMD)                 |
| 519:516                           | M   | 0x00000001    | Number of Namespaces (NN)                             |
| 521:520                           | M   | 0x005D        | Optional NVM Command Support (ONCS)                   |
| 523:522                           | M   | 0x0000        | Fused Operation Support (FUSES)                       |
| 524                               | M   | 0x00          | Format NVM Attributes (FNA)                           |
| 525                               | M   | 0x01          | Volatile Write Cache (VWC)                            |
| 527:526                           | M   | TBD           | Atomic Write Unit Normal (AWUN)                       |
| 529:528                           | M   | TBD           | Atomic Write Unit Power Fail (AWUPF)                  |
| 530                               | M   | 0x01          | NVM Vendor Specific Command Configuration (NVSCC)     |
| 531                               | -   | 0x00          | Reserved  |
| 533:532                           | O   | 0x0000        | Atomic Compare & Write Unit (ACWU)                    |
| 535:534                           | -   | 0x0000        | Reserved  |
| 539:536                           | O   | 0x00000000    | SGL Support (SGLS)                                    |
| 767:540                           | -   | 0x00          | Reserved  |
| <b>IO Command Set Attributes</b>  |     |               |   |
| 1023:768                          | M   | 0x00          | NVM Subsystem NVMe Qualified Name (SUBNQN)            |
| 1791:1024                         | -   | 0x00          | Reserved  |
| 2047:1792                         | -   | 0x00          | Reserved  |
|                                   |     |               |   |
|                                   |     |               |   |

| Bytes                  | O/M | Default Value   | Description                       |
|------------------------|-----|-----------------|-----------------------------------|
| 2079:2048              | M   | TBD             | Power State 0 Descriptor (PSD0)   |
| 2111:2080              | O   | 0x00            | Power State 1 Descriptor (PSD1)   |
| 2143:2112              | O   | 0x00            | Power State 2 Descriptor (PSD2)   |
| 2175:2144              | O   | 0x00            | Power State 3 Descriptor (PSD3)   |
| 2207:2176              | O   | 0x00            | Power State 4 Descriptor (PSD4)   |
| 2239:2208              | O   | 0x00            | Power State 5 Descriptor (PSD5)   |
| 2271:2240              | O   | 0x00            | Power State 6 Descriptor (PSD6)   |
| 2303:2272              | O   | 0x00            | Power State 7 Descriptor (PSD7)   |
| 2335:2304              | O   | 0x00            | Power State 8 Descriptor (PSD8)   |
| 2367:2336              | O   | 0x00            | Power State 9 Descriptor (PSD9)   |
| 2399:2368              | O   | 0x00            | Power State 10 Descriptor (PSD10) |
| 2431:2400              | O   | 0x00            | Power State 11 Descriptor (PSD11) |
| 2463:2432              | O   | 0x00            | Power State 12 Descriptor (PSD12) |
| 2495:2464              | O   | 0x00            | Power State 13 Descriptor (PSD13) |
| 2527:2496              | O   | 0x00            | Power State 14 Descriptor (PSD14) |
| 2559:2528              | O   | 0x00            | Power State 15 Descriptor (PSD15) |
| 2591:2560              | O   | 0x00            | Power State 16 Descriptor (PSD16) |
| 2623:2592              | O   | 0x00            | Power State 17 Descriptor (PSD17) |
| 2655:2624              | O   | 0x00            | Power State 18 Descriptor (PSD18) |
| 2687:2656              | O   | 0x00            | Power State 19 Descriptor (PSD19) |
| 2719:2688              | O   | 0x00            | Power State 20 Descriptor (PSD20) |
| 2751:2720              | O   | 0x00            | Power State 21 Descriptor (PSD21) |
| 2783:2752              | O   | 0x00            | Power State 22 Descriptor (PSD22) |
| 2815:2784              | O   | 0x00            | Power State 23 Descriptor (PSD23) |
| 2847:2816              | O   | 0x00            | Power State 24 Descriptor (PSD24) |
| 2879:2848              | O   | 0x00            | Power State 25 Descriptor (PSD25) |
| 2911:2880              | O   | 0x00            | Power State26 Descriptor (PSD26)  |
| 2943:2912              | O   | 0x00            | Power State 27 Descriptor (PSD27) |
| 2975:2944              | O   | 0x00            | Power State 28 Descriptor (PSD28) |
| 3007:2976              | O   | 0x00            | Power State 29 Descriptor (PSD29) |
| 3039:3008              | O   | 0x00            | Power State 30 Descriptor (PSD30) |
| 3071:3040              | O   | 0x00            | Power State 31 Descriptor (PSD31) |
| <b>Vendor Specific</b> |     |                 |                                   |
| 3278:3072              | O   | 0x00            | Vendor Specific (VS)              |
| 3279                   | O   | 0x00            | Vendor Specific (VS)              |
| 4095:3280              | O   | Vendor Reserved | Vendor Specific (VS)              |

\* The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at

<http://standards.ieee.org/develop/regauth/oui/public.html>.

\*\* Depends on the using of capacity

■ Identify Namespace Data Structure & NVM Command Set Specific

| Bytes   | O/M | Default Value          | Description  |
|---------|-----|------------------------|--|
| 7:0     | M   | TBD*                   | Namespace Size (NSZE)  |
| 15:8    | M   | TBD*                   | Namespace Capacity (NCAP)  |
| 23:16   | M   | TBD*                   | Namespace Utilization (NUSE)                                       |
| 24      | M   | 0x00                   | Namespace Features (NSFEAT)  |
| 25      | M   | 0x01                   | Number of LBA Formats (NLBAF)                                      |
| 26      | M   | 0x00                   | Formatted LBA Size (FLBAS)   |
| 27      | M   | 0x00                   | Metadata Capabilities (MC)   |
| 28      | M   | 0x00                   | End-to-end Data Protection Capabilities (DPC)                      |
| 29      | M   | 0x00                   | End-to-end Data Protection Type Settings (DPS)                     |
| 30      | O   | 0x00                   | Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC) |
| 31      | O   | 0x00                   | Reservation Capabilities (RESCAP)                                  |
| 32      | O   | 0x00                   | Format Progress Indicator (FPI)                                    |
| 33      | -   | 0x09                   | Reserved   |
| 35:34   | O   | 0x0000                 | Namespace Atomic Write Unit Normal (NAWUN)                         |
| 37:36   | O   | 0x0000                 | Namespace Atomic Write Unit Power Fail (NAWUPF)                    |
| 39:38   | O   | 0x0000                 | Namespace Atomic Compare & Write Unit (NACWU)                      |
| 41:40   | O   | 0x0000                 | Namespace Atomic Boundary Size Normal (NABSN)                      |
| 43:42   | O   | 0x0000                 | Namespace Atomic Boundary Offset (NABO)                            |
| 45:44   | O   | 0x0000                 | Namespace Atomic Boundary Size Power Fail (NABSPF)                 |
| 47:46   | -   | 0x0000                 | Reserved   |
| 63:48   | O   | 0x00                   | NVM Capacity (NVMCAP)  |
| 103:64  | -   | 0x00                   | Reserved   |
| 119:104 | O   | 0x00                   | Namespace Globally Unique Identifier (NGUID)                       |
| 127:120 | O   | 0x373900F0FFA779<br>64 | IEEE Extended Unique Identifier (EUI64)                            |
| 131:128 | M   | 0x02090000             | LBA Format 0 Support (LBAF0)                                       |
| 135:132 | O   | 0x00000000             | LBA Format 1 Support (LBAF1)                                       |
| 139:136 | O   | 0x00000000             | LBA Format 2 Support (LBAF2)                                       |
| 143:140 | O   | 0x00000000             | LBA Format 3 Support (LBAF3)                                       |
| 147:144 | O   | 0x00000000             | LBA Format 4 Support (LBAF4)                                       |
| 151:148 | O   | 0x00000000             | LBA Format 5 Support (LBAF5)                                       |
| 155:152 | O   | 0x00000000             | LBA Format 6 Support (LBAF6)                                       |
| 159:156 | O   | 0x00000000             | LBA Format 7 Support (LBAF7)                                       |
| 163:160 | O   | 0x00000000             | LBA Format 8 Support (LBAF8)                                       |

| Bytes   | O/M | Default Value | Description                    |
|---------|-----|---------------|--------------------------------|
| 167:164 | O   | 0x00000000    | LBA Format 9 Support (LBAF9)   |
| 171:168 | O   | 0x00000000    | LBA Format 10 Support (LBAF10) |
| 175:172 | O   | 0x00000000    | LBA Format 11 Support (LBAF11) |
| 179:176 | O   | 0x00000000    | LBA Format 12 Support (LBAF12) |
| 183:180 | O   | 0x00000000    | LBA Format 13 Support (LBAF13) |
| 187:184 | O   | 0x00000000    | LBA Format 14 Support (LBAF14) |
| 191:188 | O   | 0x00000000    | LBA Format 15 Support (LBAF15) |
| 383:192 | -   | 0x00          | Reserved                       |

\* See IDEMA SPEC

\*\* See IEEE EUI-64 SPEC

■ List of Identify Namespace Data Structure for Each Capacity

| Capacity<br>(GB) | Byte[7:0]:<br>Namespace Size (NSZE) |
|------------------|-------------------------------------|
| 240              | 1BF244B0h                           |
| 480              | 37E436B0h                           |
| 960              | 6FC81AB0h                           |
| 1920             | DF8FE2B0h                           |

### 6.3. SMART Attributes

#### ■ SMART Attributes (Log Identifier 02h)

| Bytes Index | Bytes | Description                                |
|-------------|-------|--|
| [0]         | 1     | Critical Warning                           |
| [2:1]       | 2     | Composite Temperature                      |
| [3]         | 1     | Available Spare                            |
| [4]         | 1     | Available Spare Threshold                  |
| [5]         | 1     | Percentage Used                            |
| [31:6]      | 26    | Reserved                                   |
| [47:32]     | 16    | Data Units Read                            |
| [63:48]     | 16    | Data Units Written                         |
| [79:64]     | 16    | Host Read Commands                         |
| [95:80]     | 16    | Host Write Commands                        |
| [111:96]    | 16    | Controller Busy Time                       |
| [127:112]   | 16    | Power Cycles                               |
| [143:128]   | 16    | Power On Hours                             |
| [159:144]   | 16    | Unsafe Shutdowns                           |
| [175:160]   | 16    | Media and Data Integrity Errors            |
| [191:176]   | 16    | Number of Error Information Log Entries    |
| [195:192]   | 4     | Warning Composite Temperature Time         |
| [199:196]   | 4     | Critical Composite Temperature Time        |
| [201:200]   | 2     | Temperature Sensor 1 (Current Temperature) |
| [203:202]   | 2     | Temperature Sensor 2 (N/A)                 |
| [205:204]   | 2     | Temperature Sensor 3 (N/A)                 |
| [207:206]   | 2     | Temperature Sensor 4 (N/A)                 |
| [209:208]   | 2     | Temperature Sensor 5 (N/A)                 |
| [211:210]   | 2     | Temperature Sensor 6 (N/A)                 |
| [213:212]   | 2     | Temperature Sensor 7 (N/A)                 |
| [215:214]   | 2     | Temperature Sensor 8 (N/A)                 |
| [511:216]   | 296   | Reserved                                   |

## 7. ACRONYMS



| Acronym | Definition  |
|---------|---|
| AES     | Advanced Encryption Standard                            |
| APST    | Autonomous Power State Transition                       |
| ASPM    | Active States Power Management                          |
| ATTO    | Commercial performance benchmark application            |
| CC      | Conformal Coating                                       |
| DDR     | Double Data Rate (SDRAM)                                |
| LBA     | Logical Block Addressing                                |
| MTBF    | Mean Time Between Failures                              |
| NVMe    | Non-Volatile Memory Express                             |
| OPAL    | Open Physics Abstraction Layer                          |
| PCBA    | Printed Circuit Board Assembly                          |
| PCIe    | PCI Express / Peripheral Component Interconnect Express |
| PLP     | Power Loss Protection                                   |
| PSID    | Physical Security ID                                    |
| SMART   | Self-Monitoring, Analysis and Reporting Technology      |
| TLC     | Tipple Level Cell                                       |



## 8. PART NUMBER DECODER



M2P80-ACX<sup>1</sup>X<sup>2</sup>X<sup>3</sup>X<sup>4</sup>X<sup>5</sup>X<sup>6</sup>X<sup>7</sup>X<sup>8</sup>X<sup>9</sup>

| Item   | Series    | Capacity  | NAND Flash & Temperature Grade   | PCBA           | Option                        |
|--|-----------|---|--|----------------|-------------------------------|
|  |           | X <sup>1</sup> X <sup>2</sup> X <sup>3</sup> X <sup>4</sup> X <sup>5</sup>                    | X <sup>6</sup>   | X <sup>7</sup> | X <sup>8</sup> X <sup>9</sup> |
| <b>M2P80</b>   | <b>AC</b> | <b>0240G</b> (240GB)<br><b>0480G</b> (480GB)<br><b>0960G</b> (960GB)<br><b>1920G</b> (1920GB) | <b>A</b> : 3D TLC , Standard (0°C to +70°C)<br><b>B</b> : 3D TLC , Wide (-40°C to +85°C) | See below      | See below                     |
| <p><b>X<sup>7</sup></b></p> <p><b>P</b>: Non-PLP PCBA</p> <p><b>U</b>: Support PLP PCBA</p> <p><b>X<sup>8</sup> X<sup>9</sup></b> (Reserved for specific requirement)</p> <p>Blank: Standard</p> <p><b>06</b>: Conformal Coating (CC)</p> <p><b>31</b>: AES + OPAL</p> <p><b>32</b>: AES + OPAL + PLP</p> <p><b>43</b>: AES + OPAL+ CC</p> <p><b>47</b>: AES + OPAL + PLP + CC</p> |           |   |  |                |                               |