LINEAR FLASH MEMORY CARD

SERIES-C (FxCxxx)
Product Specification

Documentation History

Version	Description	Date	Written By
1.0	New Issue	Aug. 2006	Greg Liu
2.0	Update product number definition and ordering information	Oct. 2017	Ryan Lee

Contents

Features

* PCMCIA / JEIDA standard
* Memory Capacity : 1, 2, 4MB
* Byte(x8) / word(x16) data bus selectable
* Single 5V for erase/write/read operation
* Fast access time : 150ns (maximum)
* Optional attribute memory : 8KB EEPROM
* Data polling and toggle bit feature for detection of program or erase completion
* Built-in write protect switch
* Block structure
  - 64KB / block for 8-bit operation
  - 128KB / block for 16-bit operation
* 100000 write/erase cycles per block
* Automatic erase/write
  - 1.5 second per single memory block erase
  - random-address write to previously erased byte (16 us/byte)
* Credit card size : 54.0 x 85.6 x 3.3 (mm)
* Commercial / Industrial grade

General Description

C-ONE's high performance PCMCIA series-C FLASH memory cards conform to the PCMCIA / JEIDA international standard and consist of multiple AMD's or FUJITSU's 5V only 4M bits FLASH memory devices and decoder IC mounted on a very thin printed circuit board using surface mounting technology.

This series Flash memory cards contain 16 to 128 independent device blocks. Each block can be individually erasable. To support PCMCIA-compatible byte-wide operation , the flash array is divided into 64K x 8 bits device blocks. To support PCMCIA-compatible word-wide operation , the devices are paired so that each accessible memory block is 64K words.

This series Flash memory cards offer portable , reprogrammable and nonvolatile solid-state storage media and can be used for flexible integration into various system platforms with PCMCIA/JEIDA interface. With the extra and optional 8K bytes "attribute memory" space , the Card Information Structure (CIS) can be written into it by C-ONE or by customer with standard format or customized requirements.

Product Number Definition

X1 X2 X3 X4X5X6 - X7 - X8X9

CARD Type

F: FLASH

A/M (Attribute Memory)

N: No A/M
6: With 8KB Read/Write A/M
9: With 8KB Read only A/M

Card Series

C= Series-C

Memory Capacity

001: 1MB
002: 2MB
004: 4MB

Extended Temperature

None (Commercial): 0°C~+70°C
I (Industrial): -20°C ~ +85°C
E (Extended): -40°C ~ +85°C

Data Bus

Blank field: Data bus 8bit/ 16bit selectable
08: Data bus 8bit only
16: Data bus 16bit only

Note: A/M means attribute memory

Product List

Part Number	Capacity	Attribute Memory	Description
F6C001	1MB	8KB E2PROM	1MB 8KB A/M Series C Flash Memory Card
F6C002	2MB		2MB 8KB A/M Series C Flash Memory Card
F6C004	4MB		4MB 8KB A/M Series C Flash Memory Card
F9C001	1MB	8KB E2PROM	1MB 8KB Read only A/M Series C Flash Memory Card
F9C002	2MB		2MB 8KB Read only A/M Series C Flash Memory Card
F9C004	4MB		4MB 8KB Read only A/M Series C Flash Memory Card
FNC001	1MB	None	1MB NO A/M Series C Flash Memory Card
FNC002	2MB		2MB NO A/M Series C Flash Memory Card
FNC004	4MB		4MB NO A/M Series C Flash Memory Card
F6C001-08	1MB	8KB E2PROM	1MB 8bit only 8KB A/M Series C Flash Memory Card
F6C002-08	2MB		2MB 8bit only 8KB A/M Series C Flash Memory Card
F6C004-08	4MB		4MB 8bit only 8KB A/M Series C Flash Memory Card
F9C001-08	1MB	8KB E2PROM	1MB 8bit only 8KB Read only A/M Series C Flash Memory Card
F9C002-08	2MB		2MB 8bit only 8KB Read only A/M Series C Flash Memory Card
F9C004-08	4MB		4MB 8bit only 8KB Read only A/M Series C Flash Memory Card
FNC001-08	1MB	None	1MB 8bit only NO A/M Series C Flash Memory Card
FNC002-08	2MB		2MB 8bit only NO A/M Series C Flash Memory Card
FNC004-08	4MB		4MB 8bit only NO A/M Series C Flash Memory Card
F6C001-16	1MB	8KB E2PROM	1MB 16bit only 8KB A/M Series C Flash Memory Card
F6C002-16	2MB		2MB 16bit only 8KB A/M Series C Flash Memory Card
F6C004-16	4MB		4MB 16bit only 8KB A/M Series C Flash Memory Card
F9C001-16	1MB	8KB E2PROM	1MB 16bit only 8KB Read only A/M Series C Flash Memory Card
F9C002-16	2MB		2MB 16bit only 8KB Read only A/M Series C Flash Memory Card
F9C004-16	4MB		4MB 16bit only 8KB Read only A/M Series C Flash Memory Card
FNC001-16	1MB	None	1MB 16bit only NO A/M Series C Flash Memory Card
FNC002-16	2MB		2MB 16bit only NO A/M Series C Flash Memory Card
FNC004-16	4MB		4MB 16bit only NO A/M Series C Flash Memory Card

Block Diagram

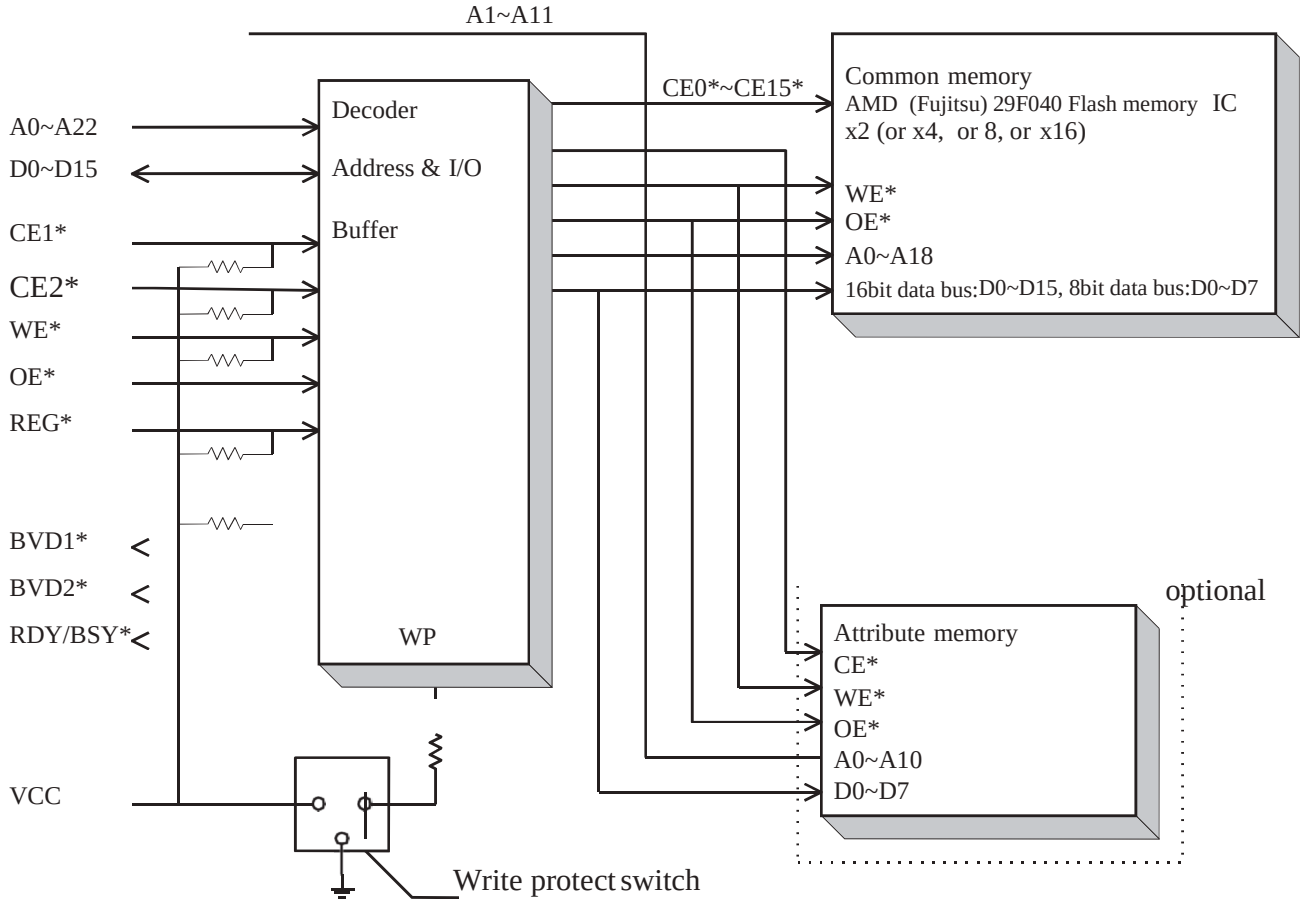


Figure 1 Cards with optional 8KB attribute memory

Pin Configuration (C1FLA08M5)

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Pin no.
VCC	RY/BY*	WE*	A14	A13	A8	A9	A11	OE*	A10	CE1*	D7	D6	D5	D4	D3	GND	Pin Name
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	Pin No.
GND	WP	D2	D1	D0	A0	A1	A2	A3	A4	A5	A6	A7	A12	A15	A16	NC	Pin Name
51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	Pin No.
VCC	A21	A20	A19	A18	A17	NC	NC	NC	CE2*	D15	D14	D13	D12	D11	CD1*	GND	Pin Name
68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	Pin No.
GND	CD2*	D10	D9	D8	BVD1*	BVD2*	REG*	NC	NC	NC	NC	NC	NC	NC	A22	NC	Pin Name

Table 2

Note :*mean low active
C1FLA02M5 series : A21,A22 = NC
C1FLA04M5 series : A22 = NC
for cards without attribute memory : pin16 , 61 = NC
8bit data bus:D8~D15=NC

Pin Description

Symbol	Function	I/O
A0-A22	Addresses	I
D0-D15	Data Inputs/Outputs	I/O
CE1*/CE2*	Card Enable	I
OE*	Output Enable	I
WE*	Write Enable	I
REG*	Attribute Memory Enable	I
WP	Write-protect status Detect	O
BVD1*/BVD2*	Battery Voltage Detect	O
RY/BY*	Ready/Busy status	O
CD1*/CD2*	Card Detect (tied to GND internally)	O
VCC	+5 Volt Power Supply	-
GND	Ground	-
NC	No Connection	-

Table 3

Pin Location

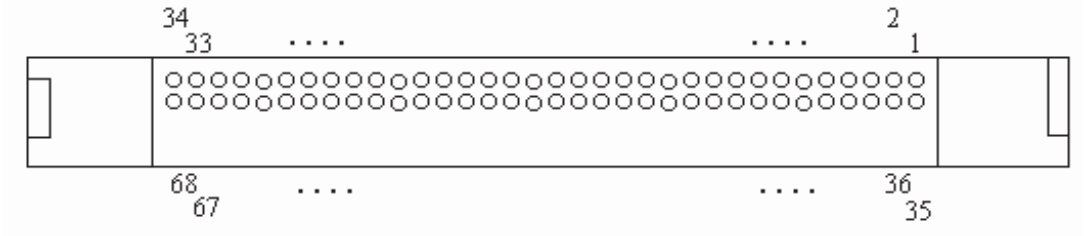


Figure 2 Bottom View (Connector Side)

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
V_{CC} Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.4	VCC + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Operating Temperature(Commercial)	T_{OPR}	0	70	° C
Operating Temperature(Industrial)	T_{OPR}	-40	85	° C

Table 4

Absolute Maximum Rating *

Parameter	Symbol	Value	Unit
V_{CC} Supply Voltage	V_{CC}	-0.5 to + 6.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}+0.3(6V max.)	V
Output Voltage	V_{OUT}	-0.5 to + 6.0	V
Operating Temperature (Commercial)	T_{OPR}	0 to + 70	□ C
Operating Temperature (Industrial)	T_{OPR}	-40 to + 85	□ C
Storage Temperature	T_{STR}	-40 to + 125	□ C
Relative Humidity (non-condensing)	H_{UM}	95(maximum)	%

Table 5

***Comments**

Stress above those listed under " Absolute Maximum Ratings " may cause permanent damage to the products. These are stress rating only. Functional operation of these products at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Common Memory Function Table

Function	REG*	CE2*	CE1*	A0	OE*	WE*	D15-D8	D7-D0
Standby	X	H	H	X	X	X	High-Z	High-Z
Byte Read	H	H	L	L	L	H	High-Z	Even Byte Data Out
	H	H	L	H	L	H	High-Z	Odd Byte Data Out
Word Read	H	L	L	X	L	H	Odd Byte Data Out	Even Byte Data Out
Odd Byte Only Read	H	L	H	X	L	H	Odd Byte Data Out	High-Z
Byte Write	H	H	L	L	H	L	X	Even Byte Data In
	H	H	L	H	H	L	X	Odd Byte Data In
Word Write	H	L	L	X	H	L	Odd Byte Data In	Even Byte Data In
Odd Byte Only Write	H	L	H	X	H	L	Odd Byte Data In	X

Table 6

Attribute Memory Function Table

Function	REG*	CE2*	CE1*	A0	OE*	WE*	D15-D8	D7-D0
Standby	X	H	H	X	X	X	High-Z	High-Z
Byte Read	L	H	L	L	L	H	High-Z	Even Byte Data Out
	L	H	L	H	L	H	High-Z	Invalid Data Out
Word Read	L	L	L	X	L	H	Invalid Data Out	Even Byte Data Out
Odd Byte Only Read	L	L	H	X	L	H	Invalid Data Out	High-Z
Byte Write	L	H	L	L	H	L	X	Even Byte Data In
	L	H	L	H	H	L	X	X
Word Write	L	L	L	X	H	L	X	Even Byte Data In
Odd Byte Only Write	L	L	H	X	H	L	X	X

Table 7

Notes :

1. L=V_{IL} ; H=V_{IH} ; X=don't care , can be either V_{IH} or V_{IL}.

Command Definition

Embedded Command Sequence	Bus Write Cycles Req	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read / Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data
Reset/Read	4	AAAAH	AAH	5554H	55H	AAAAH	F0H	RA	RD				
Autoselect	4	AAAAH	AAH	5554H	55H	AAAAH	90H	00H/02H	01H/A4H				
Byte Write	4	AAAAH	AAH	5554H	55H	AAAAH	A0H	PA	PD				
Segment Erase	6	AAAAH	AAH	5554H	55H	AAAAH	80H	AAAAH	AAH	5554H	55H	AAAAH	10H
Block Erase	6	AAAAH	AAH	5554H	55H	AAAAH	80H	AAAAH	AAH	5554H	55H	SA	30H
Block Erase Suspend		Erase can be suspended during Block erase with Addr (don't care) , Data (B0H)											
Block Erase Resume		Erase can be resumed after suspend with Addr (don't care) , Data (30H)											

Table 8 Even Byte Command Definitions

Address for Memory Segment 0 (S0) only. Address for the higher even memory segments (S2-S16) = (Addr) + (N/2) 100000H where N = Memory Segment number (0) for 1Mbyte, N = (0, 2) for 2Mbyte, N = (0, 2, 4, 6) for 4 Mbyte, N = (0...14) for 8 Mbyte.

Embedded Command Sequence	Bus Write Cycles Req	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read / Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data
Reset/Read	4	AAABH	AAH	5555H	55H	AAABH	F0H	RA	RD				
Autoselect	4	AAABH	AAH	5555H	55H	AAABH	90H	00H/02H	01H/A4H				
Byte Write	4	AAABH	AAH	5555H	55H	AAABH	A0H	PA	PD				
Segment Erase	6	AAABH	AAH	5555H	55H	AAABH	80H	AAABH	AAH	5555H	55H	AAABH	10H
Block Erase	6	AAABH	AAH	5555H	55H	AAABH	80H	AAABH	AAH	5555H	55H	SA	30H
Block Erase Suspend		Erase can be suspended during Block erase with Addr (don't care) , Data (B0H)											
Block Erase Resume		Erase can be resumed after suspend with Addr (don't care) , Data (30H)											

Table 9 Odd Byte Command Definitions

Address for Memory Segment 1 (S1) only. Address for the higher odd memory segments (S3-S15) = (Addr) + ((N-1)/2) 100000H + 80000H where N = Memory Segment number (1) for 1Mbyte, N = (1, 3) for 2Mbyte, N = (1, 3, 5, 7) for 4 Mbyte, N = (1...15) for 8 Mbyte.

Notes :

1. Address bit A16 = X = Don't Care for all address commands except for Program Address (PA), Read Address (RA) and Block Address (SA).
2. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the WE pulse.
   SA = Address of the block to be erased. The combination of A17, A18, A19 will uniquely select any block of a segment.
3. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data latched is on the rising edge of the WE pulse.

Embedded Command Sequence	Bus Write Cycles Req	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read / Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data
Reset/Read	4	AAAAH	AAAA	5554H	5555	AAAAH	F0F0	RA	RW				
Autoselect	4	AAAAH	AAAA	5554H	5555	AAAAH	9090	00H/02H	01H/A4H				
Byte Write	4	AAAAH	AAAA	5554H	5555	AAAAH	A0A0	PA	PW				
Segment Erase	6	AAAAH	AAAA	5554H	5555	AAAAH	8080	AAAAH	AAAA	5554H	5555	AAAAH	1010
Block Erase	6	AAAAH	AAAA	5554H	5555	AAAAH	8080	AAAAH	AAAA	5554H	5555	SA	3030
Block Erase Suspend		Erase can be suspended during block erase with Addr (don't care) , Data (B0H)											
Block Erase Resume		Erase can be resumed after suspend with Addr (don't care) , Data (30H)											

Table 10 Word Byte Command Definitions

Notes :

1. Address bit A16 = X = Don't Care for all address commands except for Program Address (PA), and Block Address (SA).
2. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the WE pulse.
   SA = Address of the block to be erased. The combination of A17, A18, A19 will uniquely select any block of a segment.
3. RW = Data read from location RA during read operation.(Word Mode).
   PW= Data to be programmed at location PA. Data latched is on the rising edge of the WE pulse. (Word Mode).
4. Address for Memory Segment Pair 0 (S0 and S1) only. Address for the higher odd memory segments Pair (S2, S3 = Pair 1, S4, S5 = Pair 2, S6, S7 = Pair 3 ....) is equal to (Addr) + M*(80000H) where M = Memory Segment Pair number.
5. Word = 2 bytes = odd byte and even byte.

Block	A19	A18	A17	Address Range
0	0	0	0	00000H-0FFFFH
1	0	0	1	10000H-1FFFFH
2	0	1	0	20000H-2FFFFH
3	0	1	1	30000H-3FFFFH
4	1	0	0	40000H-4FFFFH
5	1	0	1	50000H-5FFFFH
6	1	1	0	60000H-6FFFFH
7	1	1	1	70000H-7FFFFH

Note: A0 is not mapped internally

Table 11 Memory Block Address Table for Memory Segment S0

Embedded Mode Erase / Program Algorithm

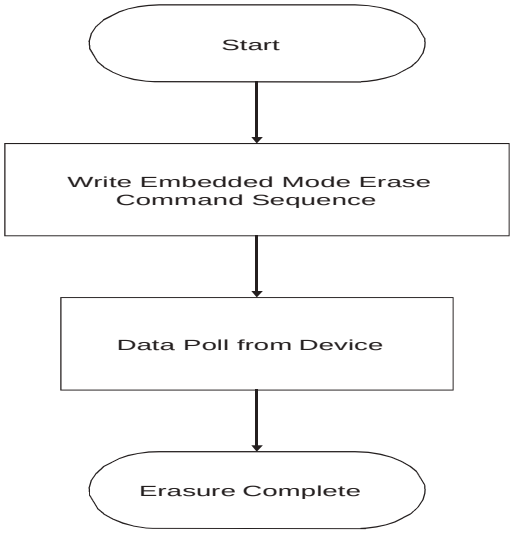


Figure 3 Embedded Mode Erase Algorithm

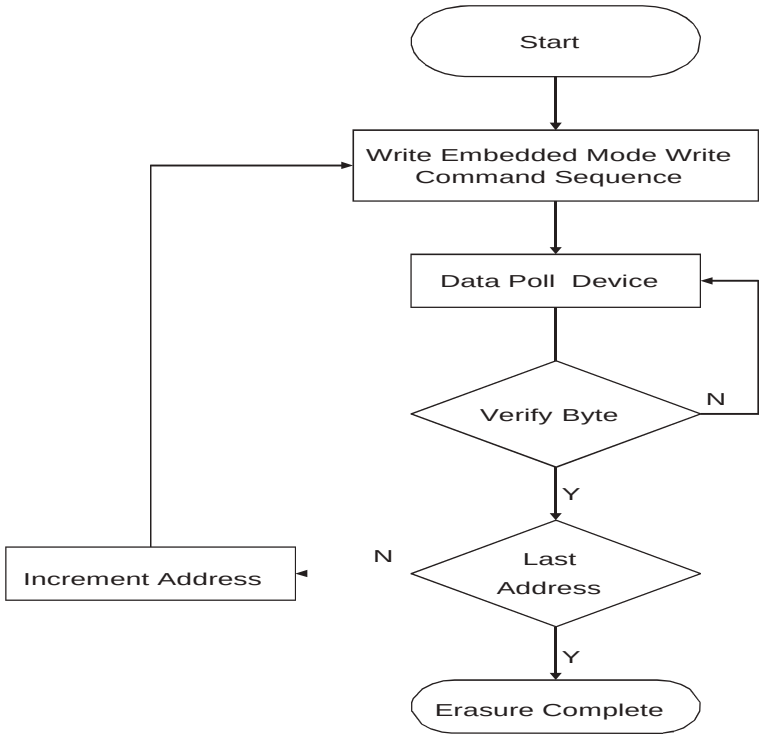


Figure 4 Embedded Mode Programing Algorithm in Byte-Wide Mode

Data Polling Algorithm

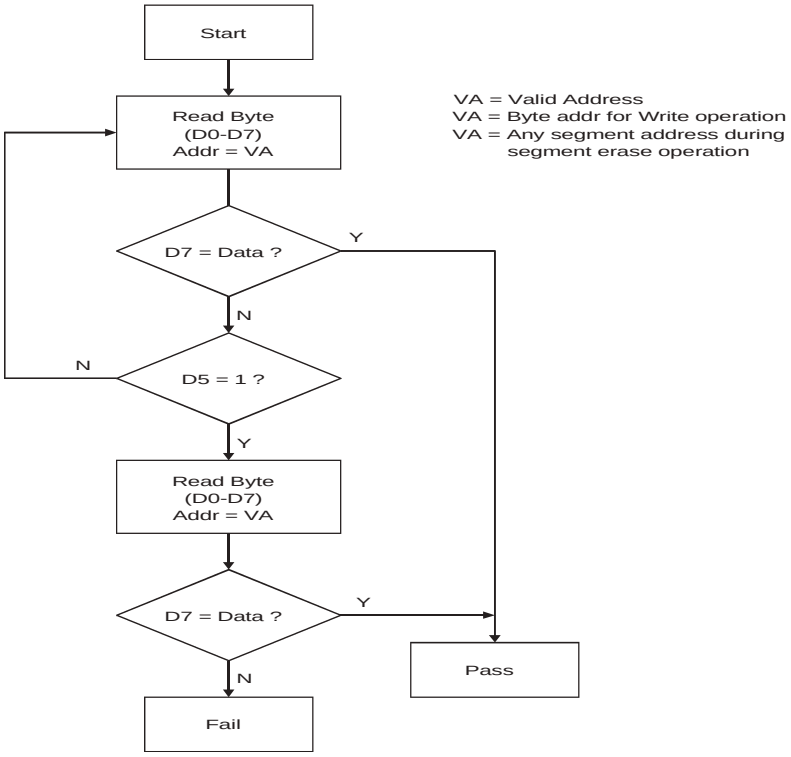
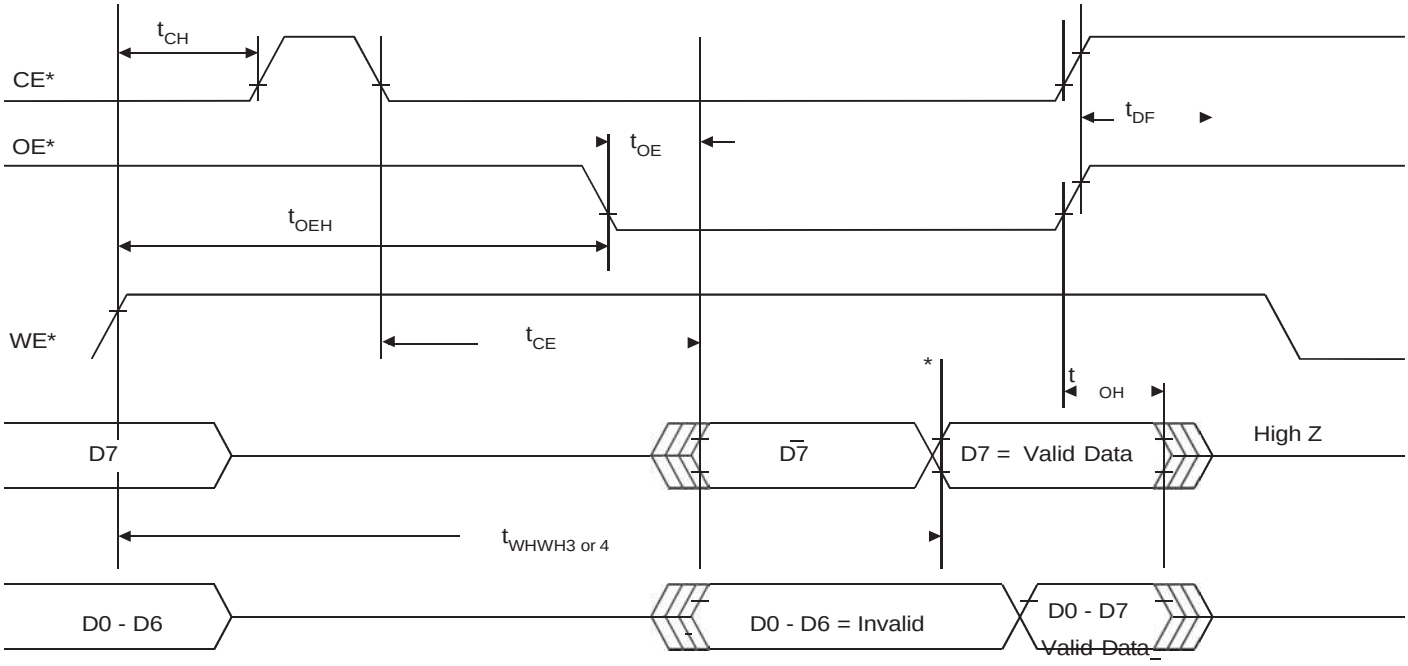


Figure 5



*D7 = Valid Data (The device has completed the Embedded operation).

Figure 6

Toggle bit Algorithm

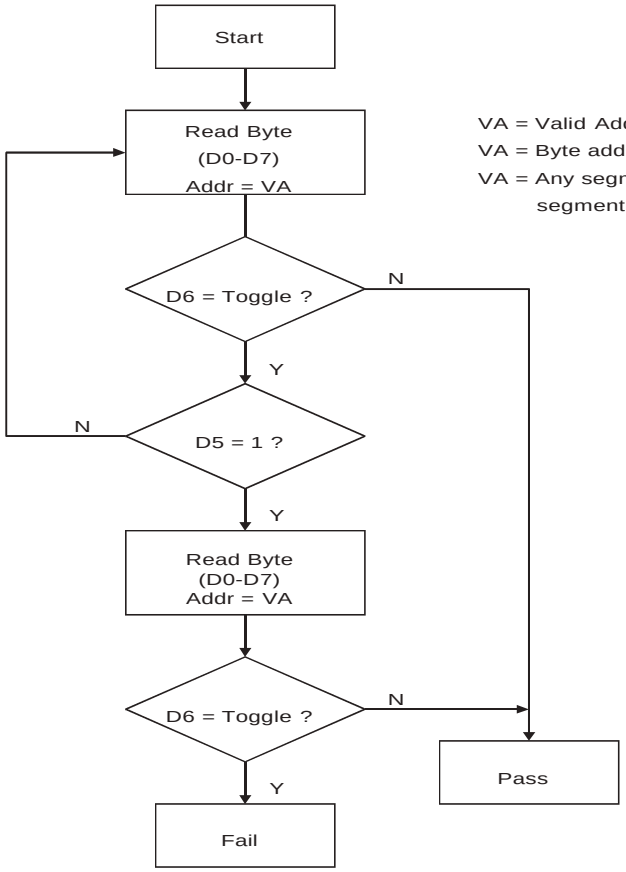
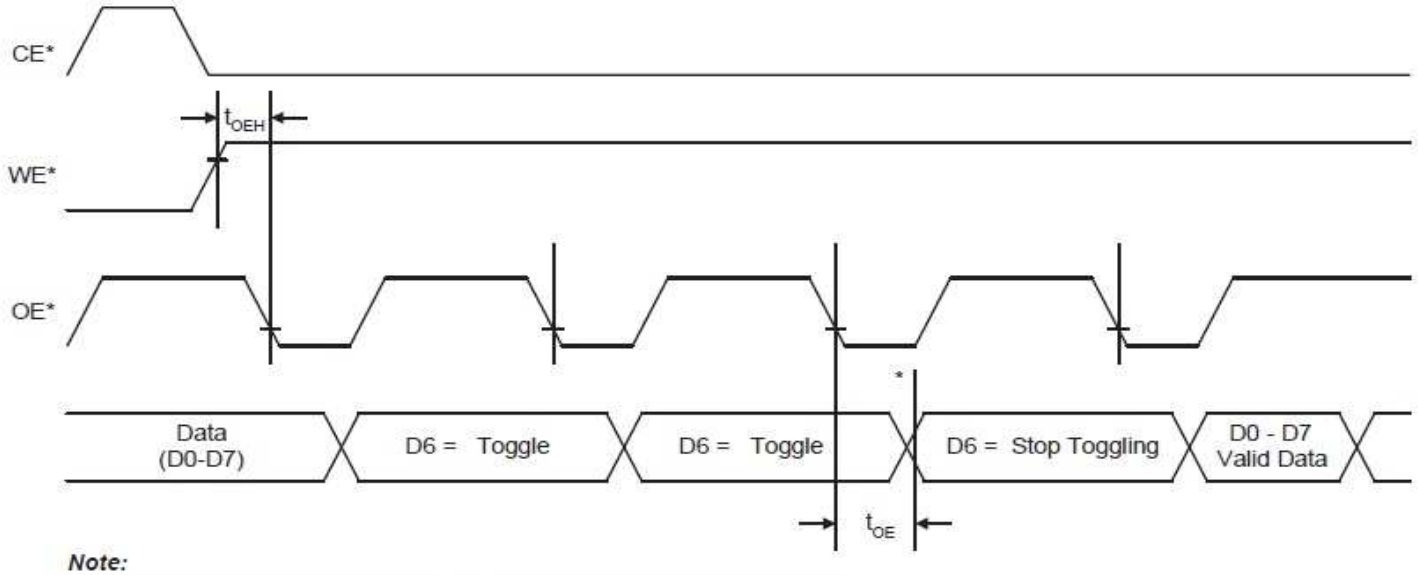


Figure 7

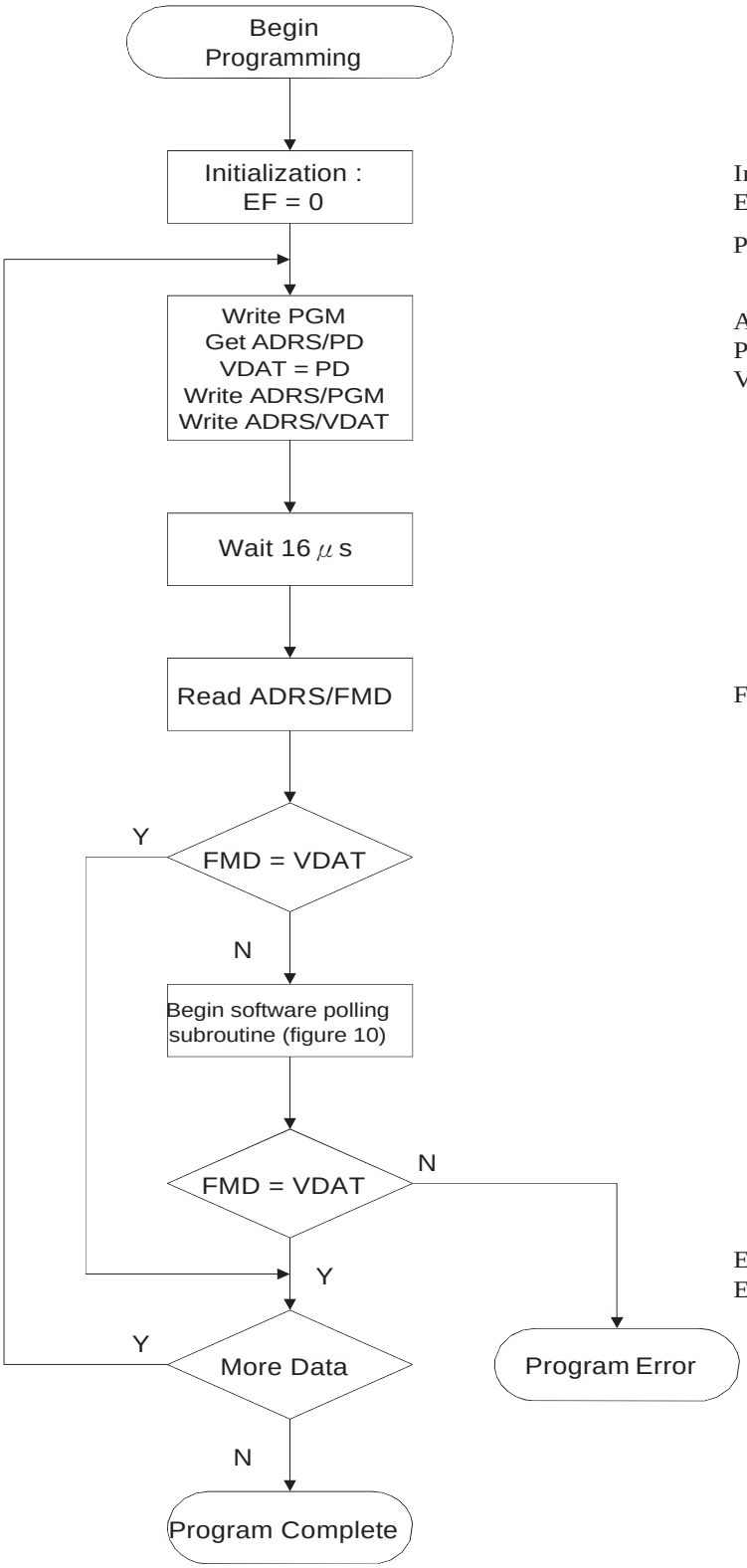


Note:

*D6 stops toggling (The device has completed the Embedded operation).

Figure 8

Byte-Wide Programming Algorithm



Initialize Programming Variables :
EF = Error Flag

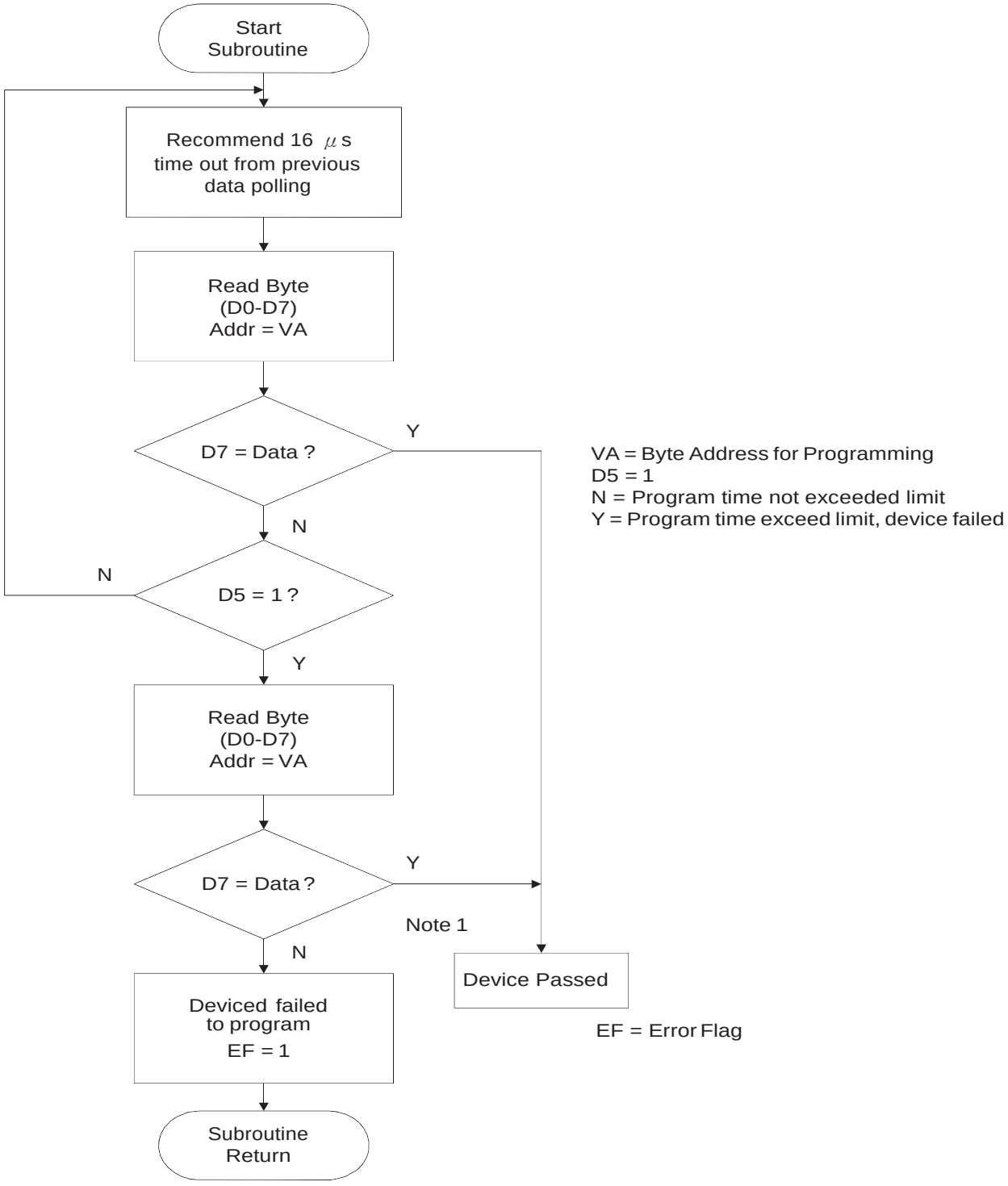
PGM = Embedded Byte Write Command Sequence Cycle #1 - #3

ADRS = Appropriate address for memory segment
PD = Program Data
VDAT = Valid Data

FMD = Flash Memory Data

EF = 0 = No Programming error
EF = 1 = Programming error

Figure 9



Note: 1. D7 is checked even if D5 = 1 because D7 may have changed simultaneously with D5 or immediately after D5.

Figure 10 Byte-wide software polling for programming subroutine

Byte-Wide erase Algorithm

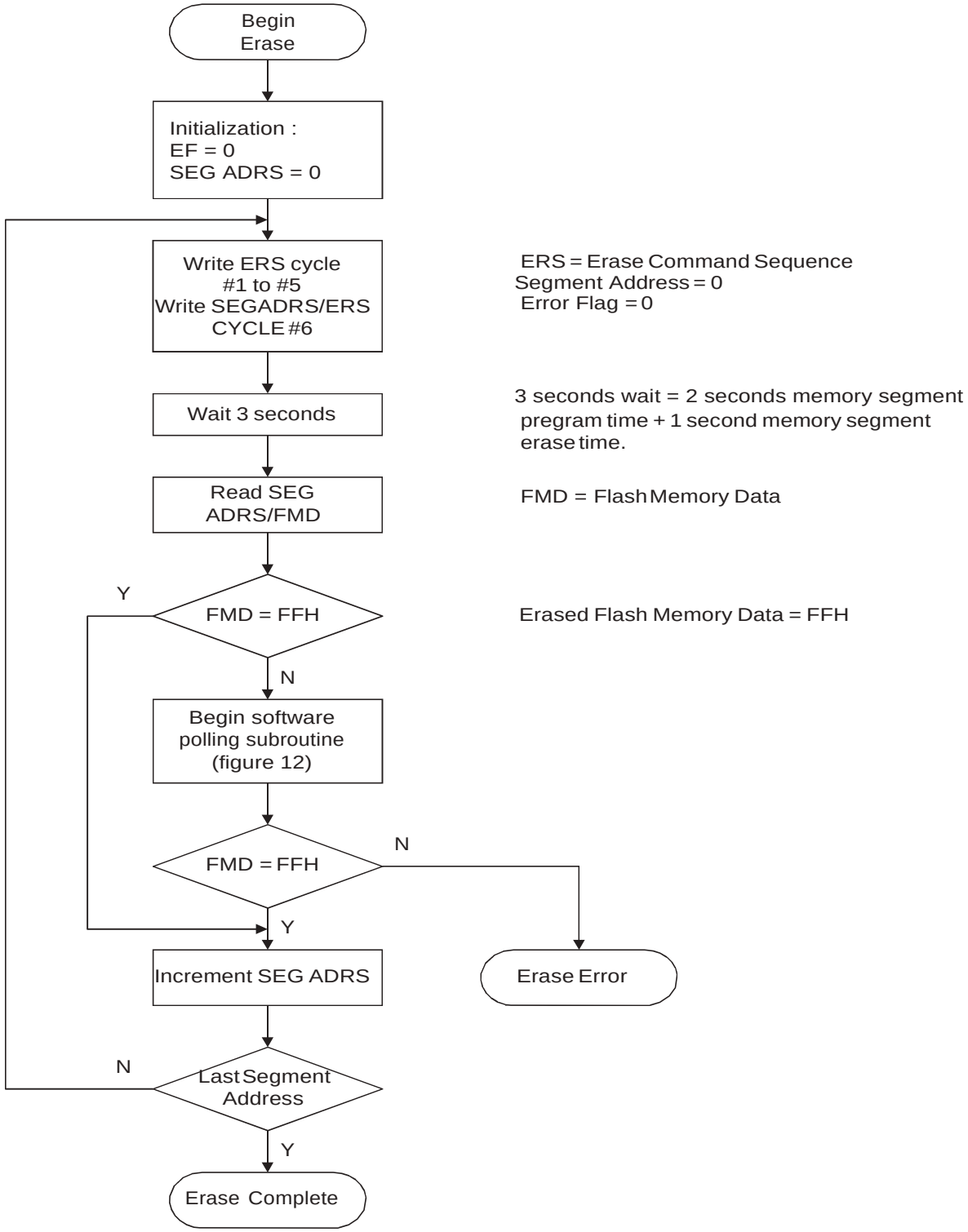


Figure 11

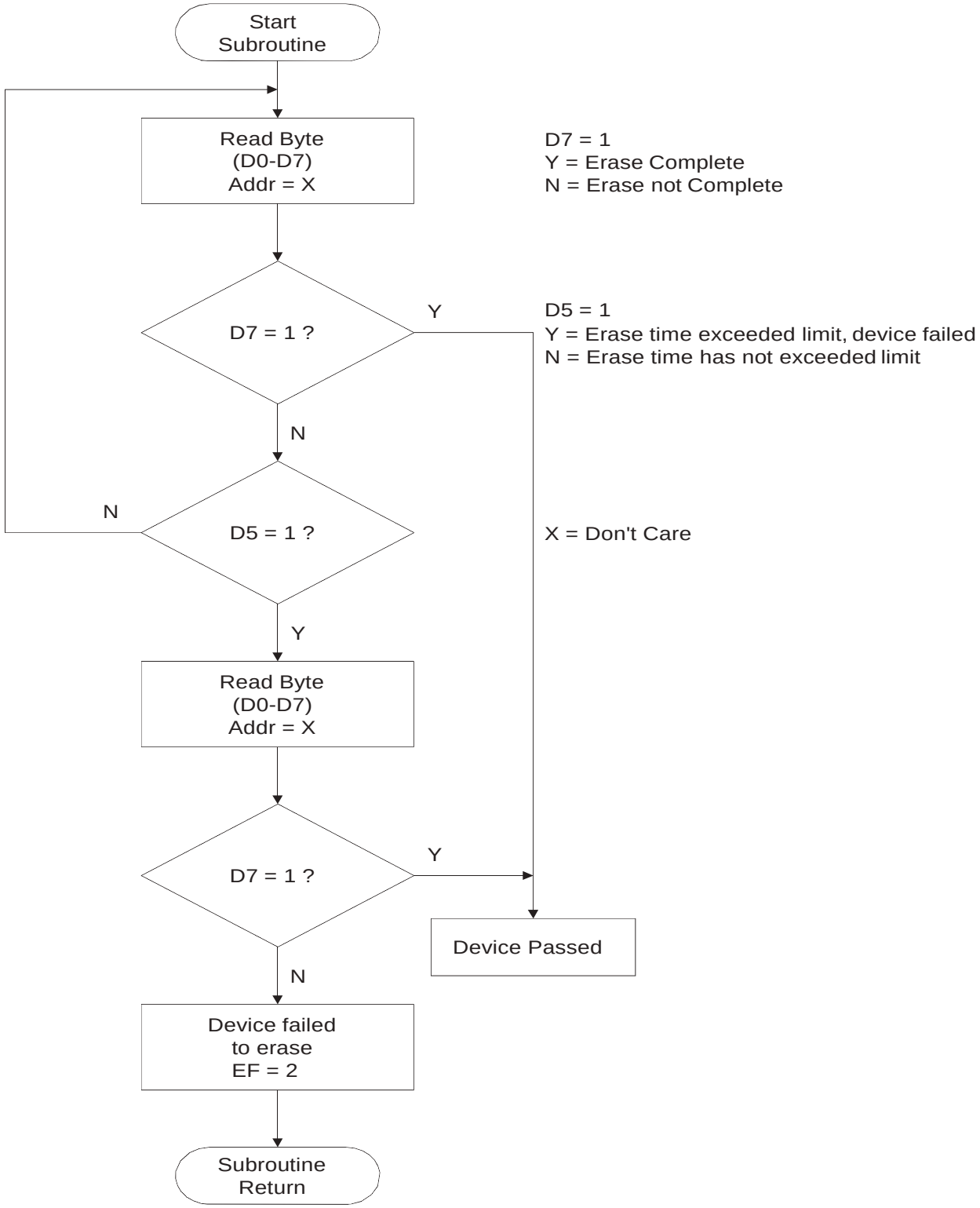


Figure 12 Byte-wide software polling erase subroutine

Word-Wide Programming Algorithm

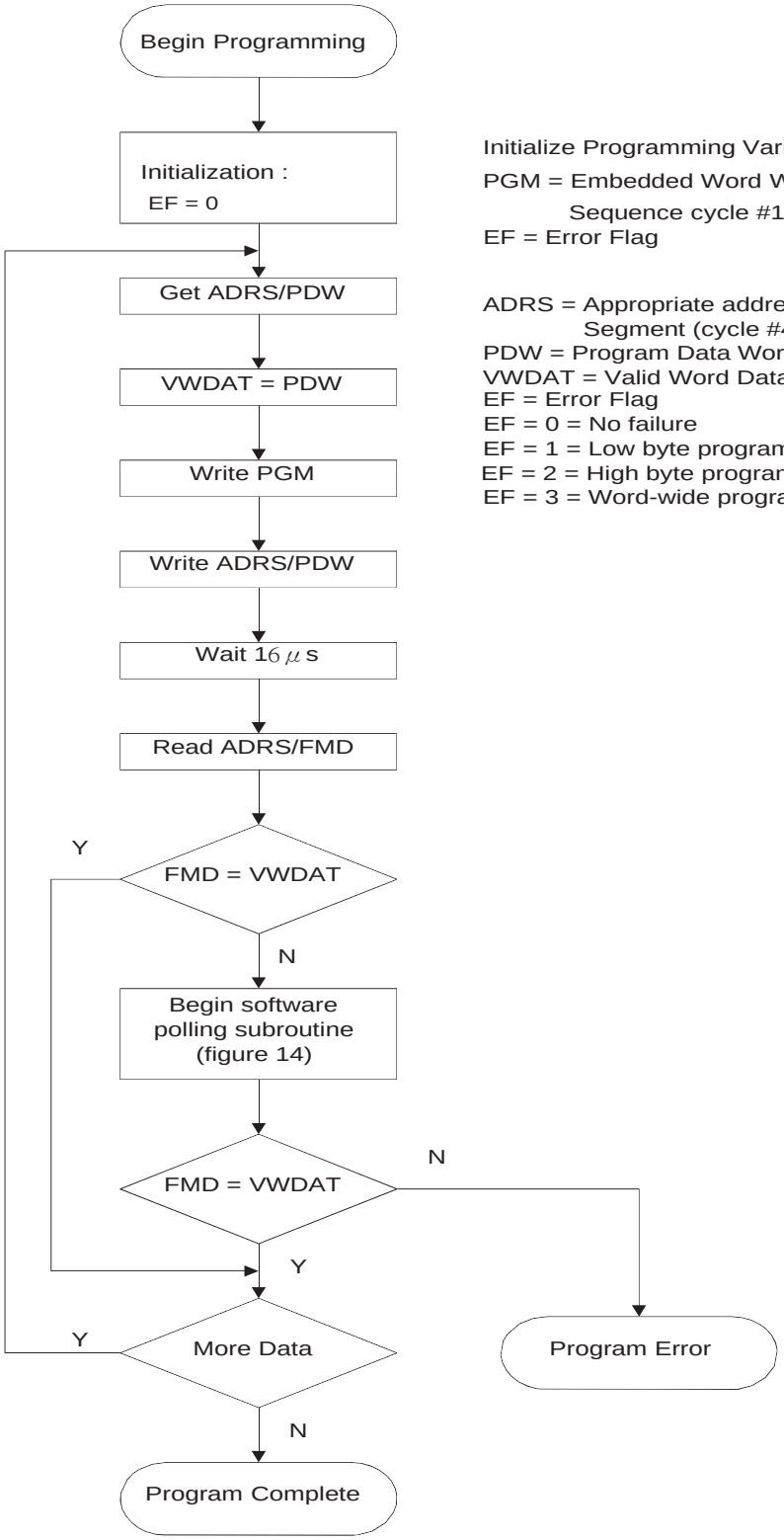


Figure 13

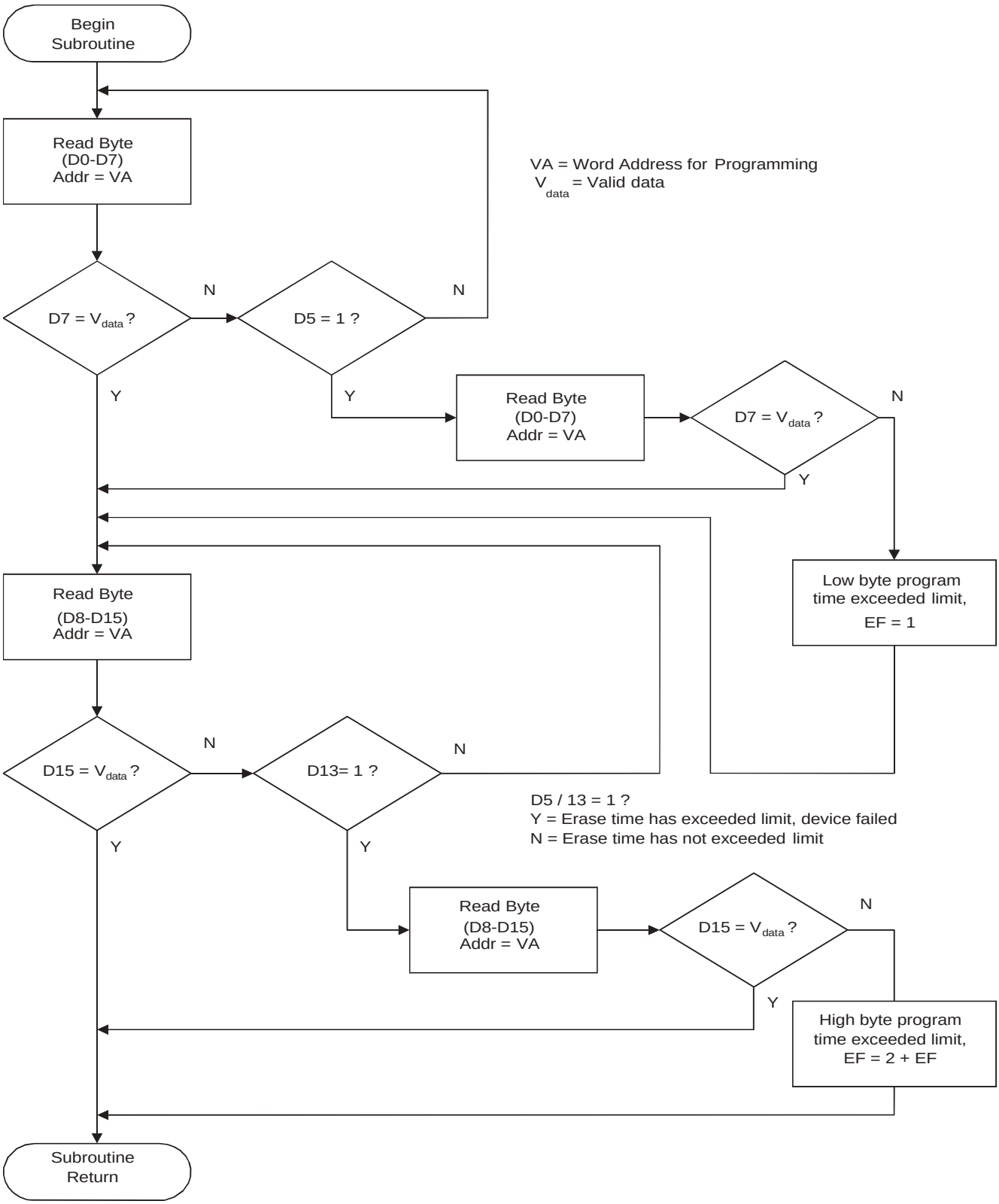


Figure 14 Word-wide software polling for programming subroutine

Word-Wide Erase Algorithm

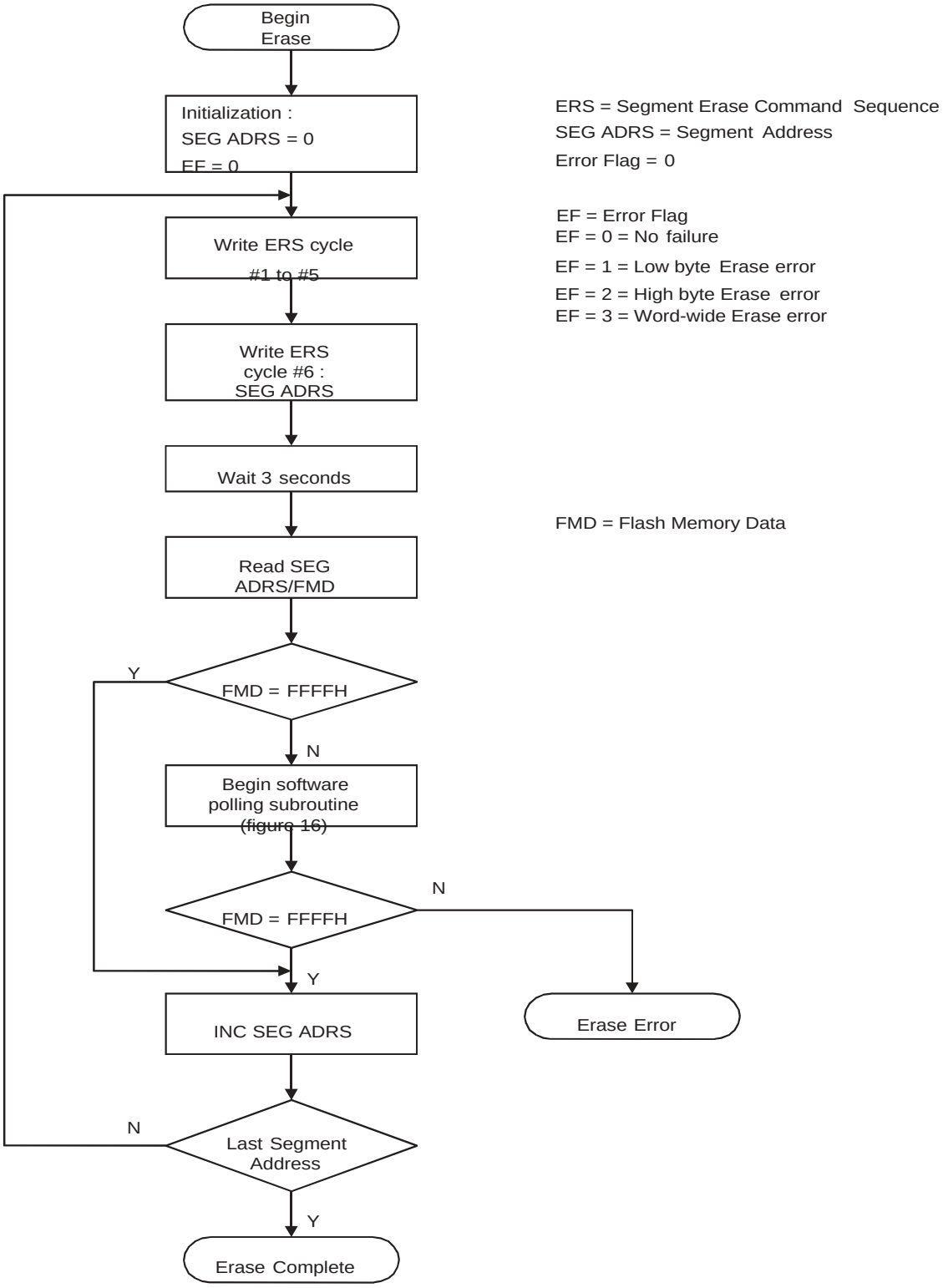


Figure 15

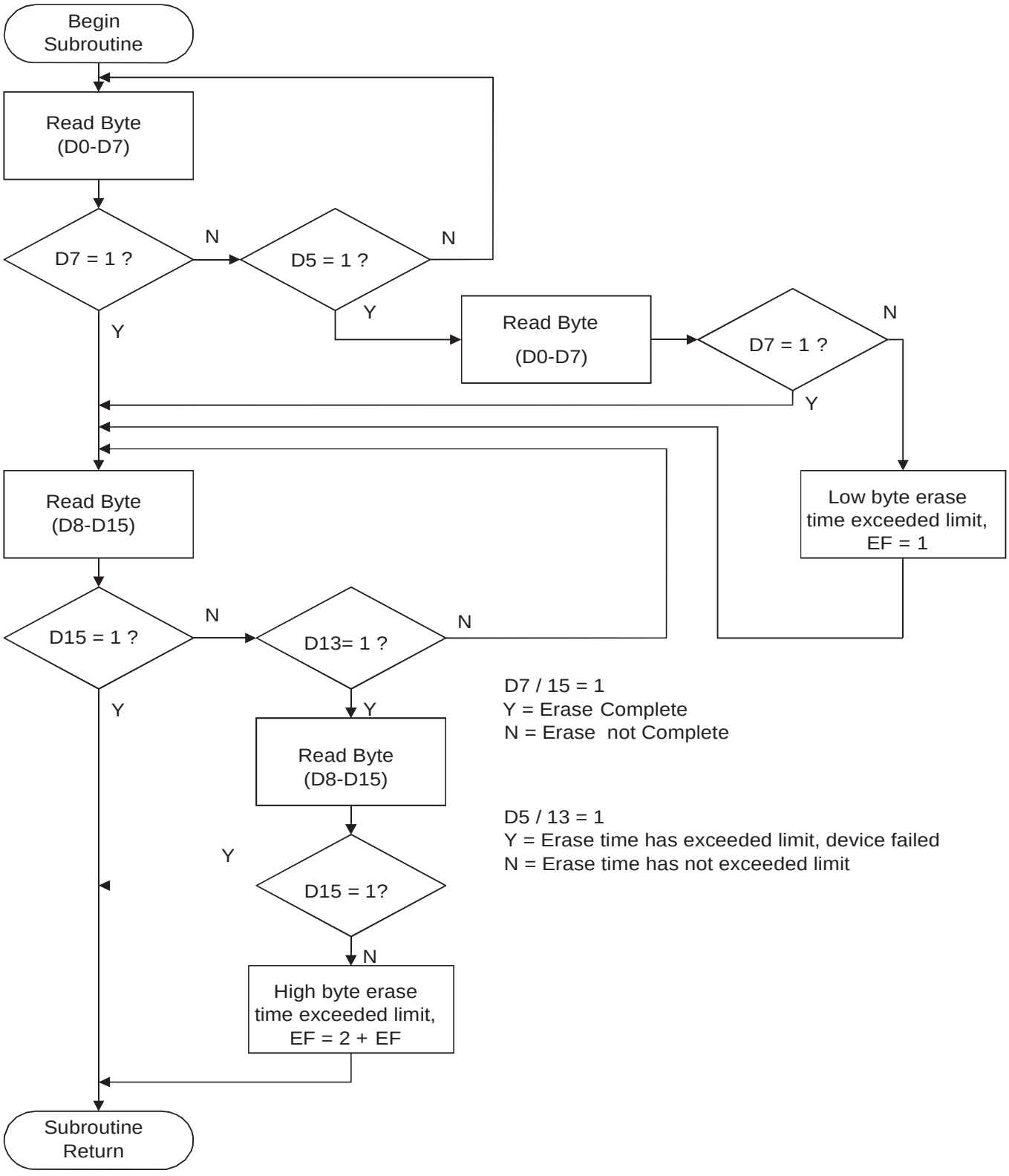


Figure 16 Word-wide software polling for erase subroutine

Tuple Information for Series-C FLASH Card

ADDRESS	DATA(Hex)	DESCRIPTION
00	01	**CISTPL_DEVICE**
02	03	TPL_LINK
04	53	FLASH card 150ns speed with WP switch
06	0D	card size = 1MB
	1D	2MB
	3D	4MB
	7D	8MB
08	FF	**END OF TUPLE LIST**
0A	15	**CISTPL_VERS_1**
0C	26	TPL_LINK
0E	04	TPLLV1_MAJOR
10	01	TPLLV1_MINOR(for PCMCIA release 2.0)
12	20	ASCII code of blank space
14	43	ASCII code of C
16	2D	ASCII code of - (dash)
18	4F	ASCII code of O
1A	4E	ASCII code of N
1C	45	ASCII code of E
1E	00	Termination of the manutacturer name
20	20	ASCII code of blank space
22	53	ASCII code of S
24	45	ASCII code of E
26	52	ASCII code of R
28	49	ASCII code of I
2A	45	ASCII code of E
2C	53	ASCII code of S
2E	2D	ASCII code of - (dash)
30	43	ASCII code of C
32	20	ASCII code of blank space
34	20	ASCII code of blank space
36	31	ASCII code of 1
	32	ASCII code of 2
	34	ASCII code of 4
	38	ASCII code of 8

ADDRESS	DATA(Hex)	DESCRIPTION
38	4D	ASCII code of M
3A	42	ASCII code of B
3C	20	ASCII code of blank space
3E	46	ASCII code of F
40	4C	ASCII code of L
42	41	ASCII code of A
44	53	ASCII code of S
46	48	ASCII code of H
48	20	ASCII code of blank space
4A	43	ASCII code of C
4C	41	ASCII code of A
4E	52	ASCII code of R
50	44	ASCII code of D
52	00	Termination of product name
54	00	Termination of lot number(no information)
56	00	Termination of programming condition
58	FF	**END OF TUPLE LIST**
5A	18	**CISTPL_JEDEC_C**
5C	02	TPL_LINK
5E	01(04)	JEDEC ID of AMD (FUJITSU)
60	A4	JEDEC ID of 29F040
62	1E	**CISTPL_DEVICE_GEO**
64	06	TPL_LINK
66	02	DGTPL_BUS
68	11	DGTPL_EBS
6A	01	DGTPL_RBS
6C	01	DGTPL_WBS
6E	01	DGTPL_PART=1
70	01	DGTPL_HWIL=1(non-interleaved card)
72	21	**CISTPL_FUNCID**
74	02	TPL_LINK
76	01	TPLFID_ FUNCTION(PC Card is memory card)
78	00	TPLFID_SYSINIT (none)
7A	FF	**CISTPL_END**
7C	FF	END

DC Electrical Characteristics

(recommended operating conditions unless otherwise noted)

Symbol	Parameter	8-Bit Mode		16-Bit Mode		Unit	Test Condition
		min	max	min	max		
I_{LI}	Input Leakage Current	-10	10	-10	10	uA	V_{IN} = 0V to V_{CC} (Note 1)
		-70	10	-70	10	uA	V_{IN} = 0V to V_{CC} (Note 2)
I_{LO}	Output Leakage Current	-10	10	-10	10	uA	CE1* = CE2* = V_{IH} or OE* = V_{IH} , V_{OUT} = 0V to V_{CC} (Note 3)
V_{IH}	Input High Voltage	2.4	V_{CC}+0.3	2.4	V_{CC}+0.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	-0.3	0.8	V	
V_{OH}	Output High Voltage	3.8		3.8		V	I_{OH} = -2.0mA (Note 4)
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 3.2mA (Note 4)
I_{CCR}	V_{CC} Read Current		45		90	mA	Min. cycle , I_{OUT} = 0mA
I_{CCW}	V_{CC} Write /Erase Current		65		130	mA	Write/erase in progress

Table 12

Note : 1.) Except CE1* , CE2* , WE* , REG* pins.

2.) For CE1* , CE2* , WE* , REG* pins.

3.) Except BVD1* , BVD2* , CD1* , CD2* pins.

4.) Except CD1* , CD2* pins.

AC Electrical Characteristics

(recommended operating conditions unless otherwise noted)

Read Cycle (Common Memory)

Symbol		Parameter	Min	Max	Unit	Notes
t_{AVAV}	t_{RC}	Read Cycle Time	150		ns	
t_{ELQV}	t_{CE}	Card Enable Access Time		150	ns	
t_{AVQV}	t_{ACC}	Address Access Time		150	ns	
t_{GLQV}	t_{OE}	Output Enable Access Time		75	ns	
t_{ELQX}	t_{LZ}	Card Enable to Output in Low-Z	5		ns	
t_{EHQZ}	t_{DF}	Card Disable to Output in High-Z		75	ns	
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low-Z	5		ns	
t_{GHQZ}	t_{DF}	Output Disable to Output in High-Z		75	ns	
t_{AXQX}	t_{OH}	Output Hold From First of Address, CE*, or OE* Change	5		ns	
t_{WHGL}		Write Recovery Time Before Read	6		μs	

Table 13

Write/Erase Cycle (Common Memory)

Symbol		Parameter	Min	Max	Unit	Notes
t_{AVAV}	t_{WC}	Write Cycle Time	150		ns	
t_{AVWL}	t_{AS}	Address Setup Time	20		ns	
t_{WLAX}	t_{AH}	Address Hold Time	55		ns	
t_{DVWH}	t_{DS}	Data Setup Time	50		ns	
t_{WHDX}	t_{DH}	Data Hold Time	20		ns	
t_{OEH}		Output Enable Hold Time for Embedded Algorithm	20		ns	
t_{WHGL}	t_{WR}	Write Recovery Time before Read	6		μs	
t_{GHWL}		Read Recovery Time before Write	0		μs	
t_{WLOZ}		Output in High-Z from Write Enable	5		ns	
t_{WHOZ}		Output in Low-Z from Write Enable		60	ns	
t_{ELWL}	t_{CS}	CE* Setup Time	0		us	
t_{WHEH}	t_{CH}	CE* Hold Time	20		sec	
t_{WLWH}	t_{WP}	Write Pulse Width	45		ns	
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	50		ns	
t_{WHWH3}		Embedded Mode Programming Operation	48		ms	1
t_{WHWH4}		Embedded Mode Erase Operation for each 64K Byte Memory Block			s	2
t_{VCS}		V_{CC} Setup Time CE* LOW			μs	3

Table 14

Note: 1. 16 μs typical 2. 1.5 seconds typical 3. 50 μs typical

Write/Erase Cycle (Common Memory) (CE* Controlled)

Symbol		Parameter	Min	Max	Unit	Notes
t_{AVAV}	t_{WC}	Write Cycle Time	150		ns	
t_{AVEL}	t_{AS}	Address Setup Time	20		ns	
t_{ELAX}	t_{AH}	Address Hold Time	55		ns	
t_{DVEH}	t_{DS}	Data Setup Time	50		ns	
t_{EHDX}	t_{DH}	Data Hold Time	20		ns	
t_{GLDV}	t_{OE}	Output Enable Hold Time for Embedded Algorithm	20		ns	
t_{GHEL}		Read Recovery Time before Write	0		μs	
t_{WLEL}	t_{WS}	WE* Setup Time before CE*	0		ns	
t_{EHWH}	t_{WH}	WE* Hold Time	0		ns	
t_{ELEH}	t_{CP}	CE* Pulse Width	65		ns	
t_{EHEL}	t_{CPH}	CE* Pulse Width HIGH	50		ns	
t_{EHEH3}		Embedded Mode Programming Operation	16		μs	
				48	ms	
t_{EHEH4}		Embedded Mode Erase Operation for each 64K Byte Memory Block	1.5		s	
t_{VCS}		V_{CC} Setup Time To Write Enable LOW	50		μs	

Table 15

Read Cycle Timing Diagram (Common Memory)

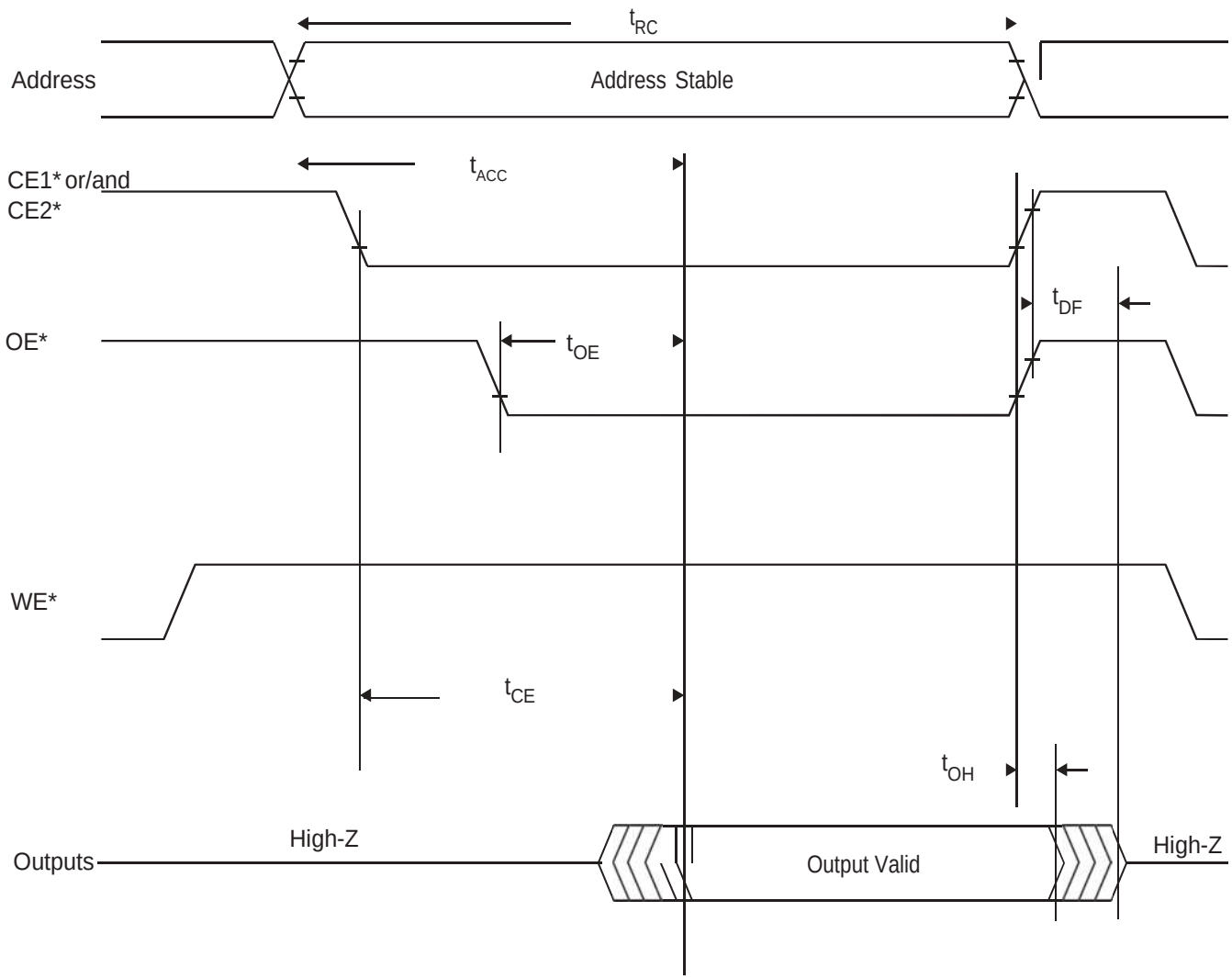


Figure 17

Write Cycle Timing Diagram (Common Memory)

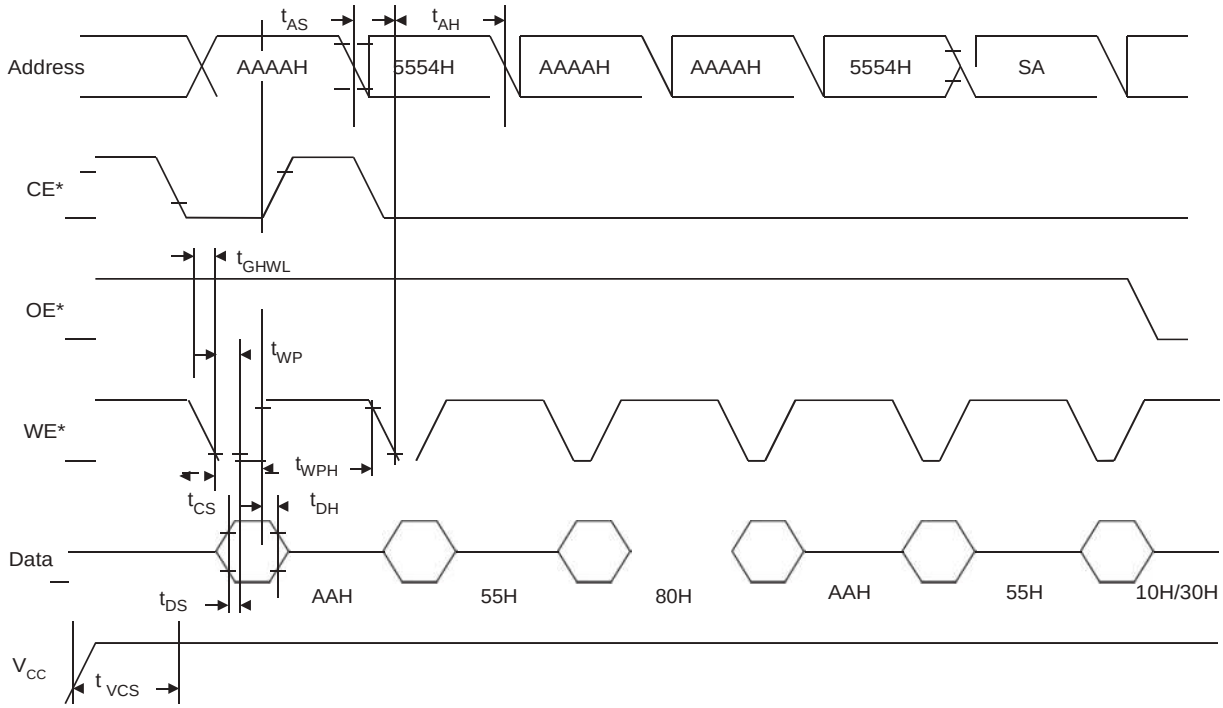
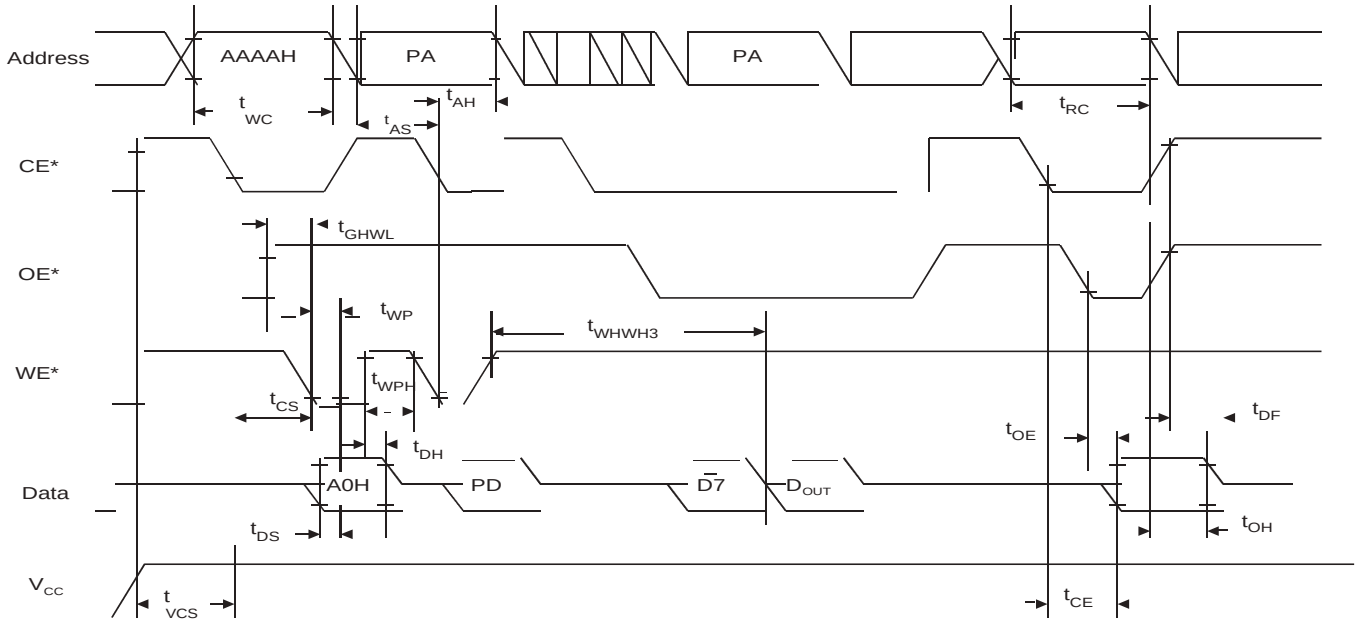


Figure 18 Segment / Block byte erase



Notes :
1. Figure indicates last two bus cycles of four bus cycle sequence.
2. PA is address of the memory location to be programmed.
3. PD is data to be programmed at byte address.
4. $\bar{D}7$ is the output of the complement of the data written to the device.
5. D_{OUT} is the output of the data written to the device.

Figure 19 Byte write

AC Electrical Characteristics (Attribute Memory)

(recommended operating conditions unless otherwise noted)

Read Cycle (Attribute Memory)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{cr}	Read Cycle Time	300		ns	
$t_a(A)$	Address Access Time		300	ns	
$t_a(CE)$	Card Select Access Time		300	ns	
$t_a(OE)$	Output Enable Access Time		150	ns	
$t_{dis}(CE)$	Output Disable Time (from CE*)		100	ns	
$t_{dis}(OE)$	Output Disable Time (from OE*)		100	ns	
$t_{en}(CE)$	Output Enable Time (from CE*)	5		ns	
$t_{en}(OE)$	Output Enable Time (from OE*)	5		ns	
$t_v(A)$	Data Hold Time (from address changed)	0		ns	

Table 16

Write Cycle (Attribute Memory)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
$t_{\mathbf{CW}}$	Write Cycle Time		1	ms	
$t_{\mathbf{AS}}$	Address Setup Time	30		ns	
$t_{\mathbf{AH}}$	Address Hold Time	50		ns	
$t_{\mathbf{WP}}$	Write Pulse Width	120		ns	
$t_{\mathbf{CS}}$	Card Enable Time to WE*	15		ns	
$t_{\mathbf{CH}}$	Card Enable Hold Time from WE* High	0		ns	
$t_{\mathbf{DS}}$	Data Setup Time	70		ns	
$t_{\mathbf{DH}}$	Data Hold Time	30		ns	
$t_{\mathbf{OES}}$	OE* Setup Time	30		ns	
$t_{\mathbf{OEH}}$	OE* Hold Time	30		ns	

Table 17

Read Cycle Timing Diagram (Attribute Memory) (REG*=VIL , WE*=VIH)

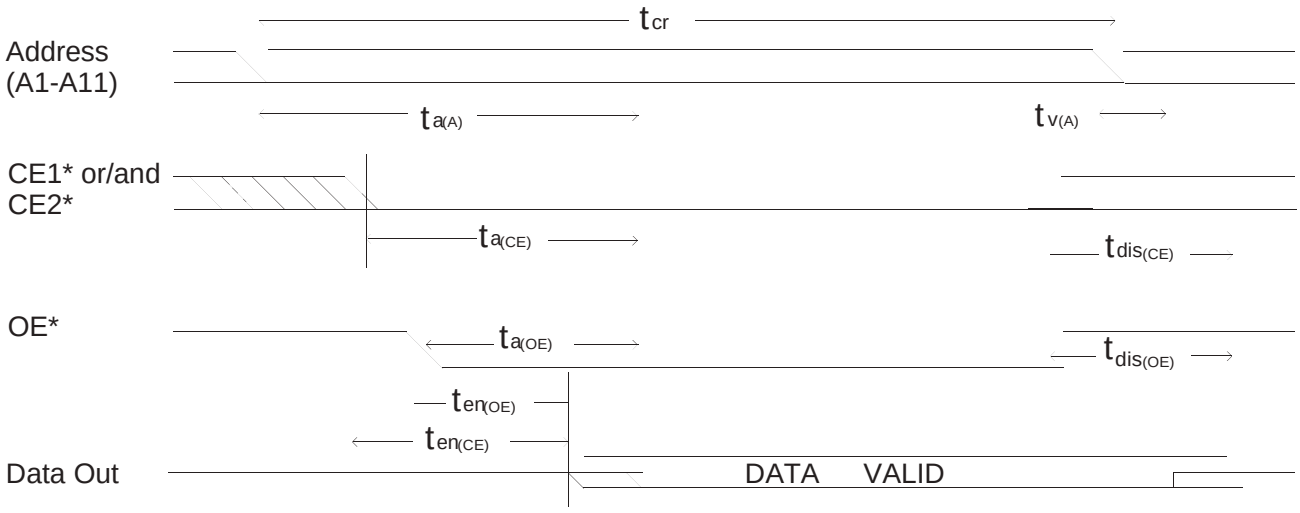


Figure 20

Write Cycle Timing Diagram (Attribute Memory) (REG*=VIL)

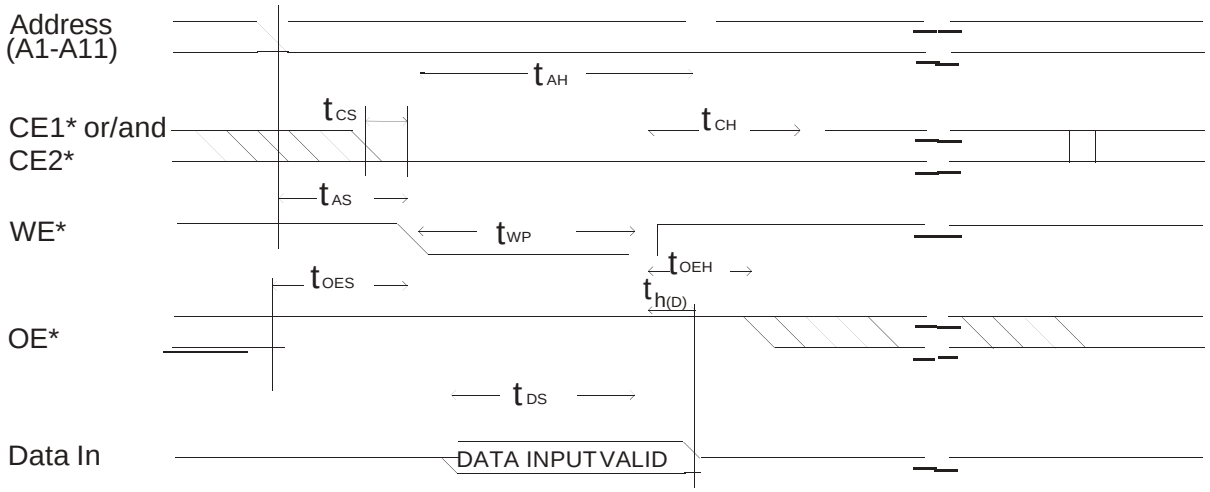
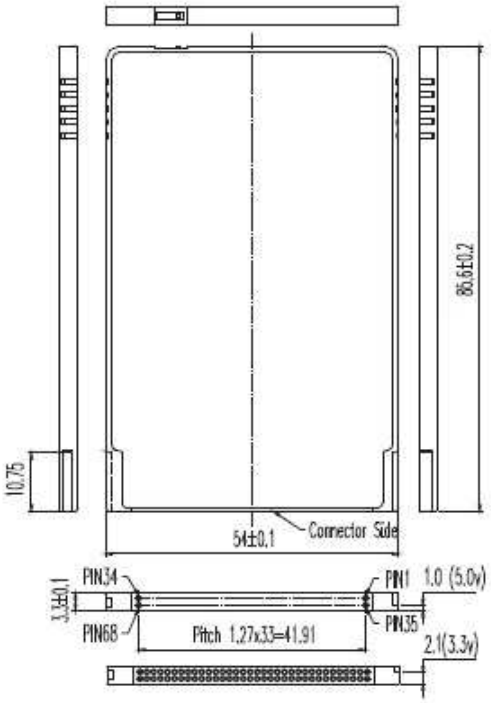
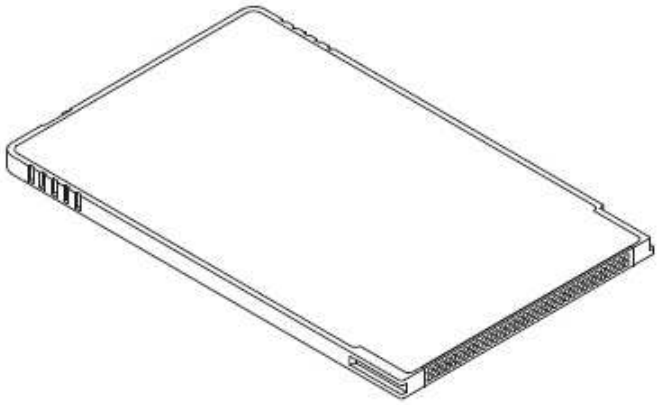


Figure 21

Outline Dimensions (Unit : mm)





FLASH CARD (Write Protect)