APRO Co., Ltd.

October 2013

Product Specification
SLC (Rugged Metal) CompactFlash Card
- HERCULES-N Series-

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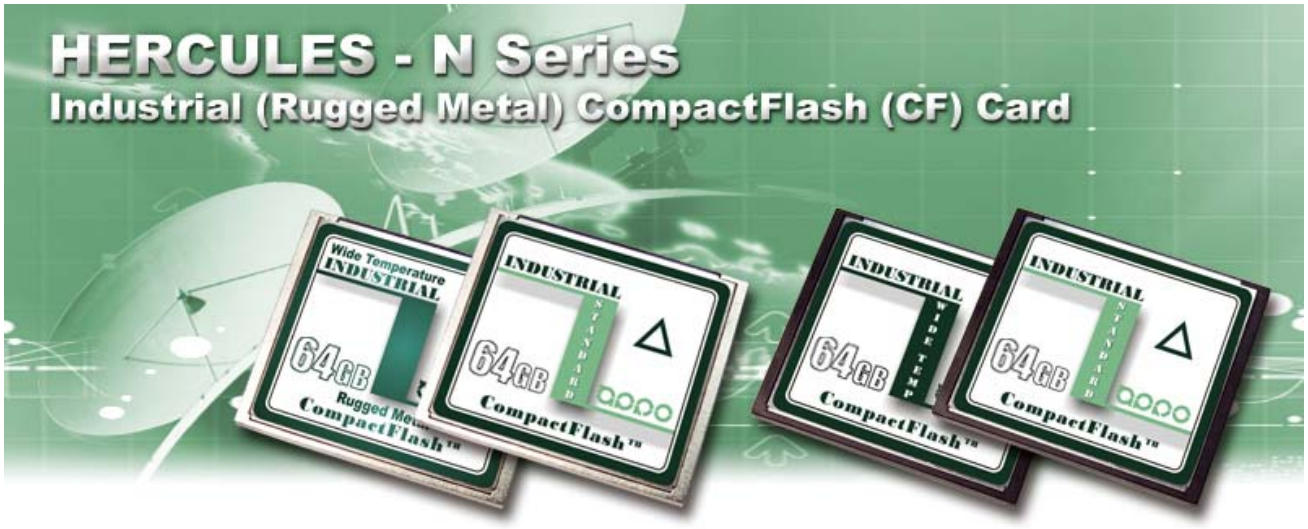

Revision History

Revision	*Description*	*Date*
1.0	*Initial Release*	*2013/10/01*

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1. Introduction

APRO industrial CompactFlash (CF) Card HERCULES-N Series designed to follow ATAPI-8 standard and fully compatible with CompactFlash® specification version 6.0. The main used Flash memories are SLC-NAND type flash memory chips. The available Card capacities are 2GB, 4GB, 8GB, 16GB, 32GB and 64GB. The operating temperature grade is optional for commercial level 0°C ~ 70°C and wide temperature level -40°C ~ +85°C. The APRO industrial CompactFlash (CF) Cards are designed electrically complies with the conventional IDE hard Card and support True IDE Mode. The data transfer modes supports PIO- 0~6 or MWDMA- 0~4 or UDMA- 0~7. The fastest reading speed is up to 113.5 MB/sec and writing speed is up to 83.8 MB/sec.

The APRO industrial CF products provide a high level interface to the host computer. This interface allows a host computer to issue commands to the CompactFlash (CF) Card to read or write blocks of memory. Each sector is protected by a powerful 72 bits per 1024 bytes block Error Correcting Code (ECC). APRO industrial CompactFlash (CF) Card's HERCULES-N Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management and clock control.

Figure 1 shows a block diagram of the used high tech CompactFlash (CF) Card controller.

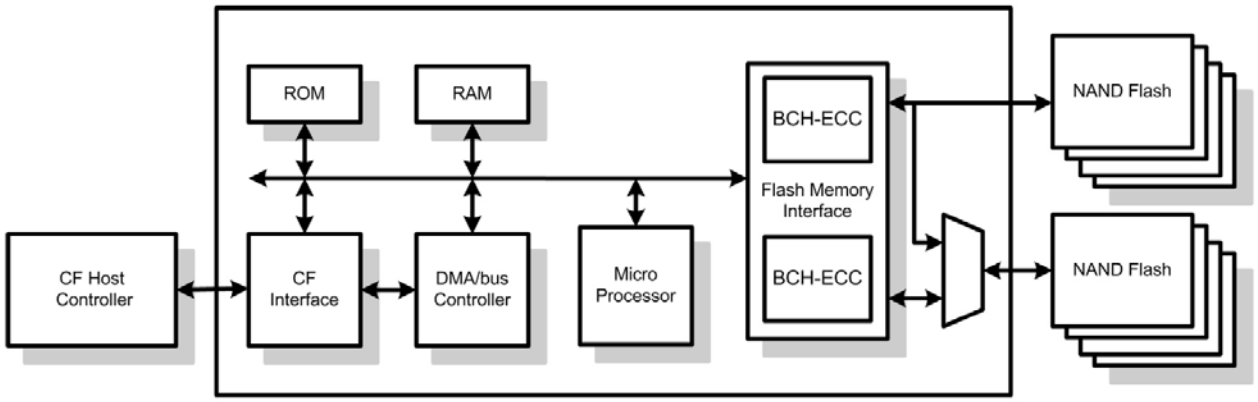

Figure 1: CompactFlash Card HERCULES-N Series Controller Block Diagram

1.1. *Scope*

This document describes the features and specifications and installation guide of APRO industrial CompactFlash (CF) Card HERCULES-N Series. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

1.2. *System Features*

- Non-volatile memory and no moving parts
- NAND type SLC flash technology
- Card capacity from 2GB to 64GB
- ATA inter face and support PC Card Memory mode, PC Card I/O mode and True IDE mode
- Data transfer supports PIO- 0~6, MWDMA- 0~4 or UDMA- 0~7
- The fastest reading speed is up to 113.5 MB/sec and writing speed is up to 83.8 MB/sec
- 72 bits per 1024 bytes block error correction (ECC) and retry capabilities
- Supports S.M.A.R.T. function (Self-Monitoring, Analysis and Reporting Technology)
- +5 V ±10% or +3.3 V ±5% operation
- Shock : 1,500 compliance to MIL-STD-810F
- Vibration : 15G compliance to MIL-STD-810F
- Working well in severe environment
- Supports Auto Stand-by mode and Auto Sleep mode
- Very high performance, very low power consumption
- Low weight, Noiseless

1.3. *CFA 6.0 Specification*

APRO industrial CompactFlash (CF) Card HERCULES-N Series is fully compatible with the CompactFlash® specification version 6.0.

1.4. *ATA/ATAPI-8 Standard*

APRO industrial CompactFlash (CF) Card HERCULES-N Series is compliant to ATA/ATAPI-8 and below version.

1.5. *Technology Independence*

With the proprietary method to manage variable kinds of flash in terms of global wear-leveling and 72 bits per 1024 bytes block ECC (Error Code Correction), it translate the ATA control, address and data bus signals into the management unit of NAND type flash devices and constitute the CompactFlash (CF) Cards more ideal than the conventional hard Card drives.

Conformal coating

Conformal coating is a protective, dielectric coating designed to conform to the surface of an assembled printed circuit board. Commonly used conformal coatings include silicone, acrylic, urethane and epoxy. APRO applies only silicone on APRO storages products upon requested especially by customers. The type of silicone coating features good thermal shock resistance due to flexibility. It is also easy to apply and repair.

Conformal coating offers protection of circuitry from moisture, fungus, dust and corrosion caused by extreme environments. It also prevents damage from those Flash storages handling during construction, installation and use, and reduces mechanical stress on components and protects from thermal shock. The greatest advantage of conformal coating is to allow greater component density due to increased dielectric strength between conductors.

APRO uses MIL-I-46058C silicon conformal coating.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. *System Environmental Specifications*

Table 1: Environmental Specification

CompactFlash (CF) Card HERCULES-N Series		**Commercial Grade**	**Industrial Grade**
Temperature	**Operating:**	0ºC ~ +70ºC	-40ºC ~ +85ºC
	Non-operating:	-20ºC ~ +80ºC	-50ºC ~ +95ºC
Humidity	**Operating & Non-operating:**	10% ~ 95% non-condensing	
Vibration	**Operating & Non-operating:**	15G compliance to MIL-STD-810F	
Shock	**Operating & Non-operating:**	1,500G compliance to MIL-STD-810F	

2.2. *System Power Requirements*

Table 2: Power Requirement

CompactFlash (CF) Card HERCULES-N Series		**Commercial Grade**	**Industrial Grade**
DC Input Voltage (VCC) 100mV max. ripple(p-p)		**+5V ± 10% / +3.3V ± 5%**	
+5V Current (Maximum average value)	**Reading Mode :**	210 mA (Typ.)	
	Writing Mode :	210 mA (Typ.)	
	Idle Mode :	6.6 mA (Typ.)	

2.3. *System Performance*

Table 3: System Performances

Data Transfer Mode supporting			- PIO mode : 0, 1, 2, 3, 4, 5, 6 - DMA SW Mode: Not supported - DMA MW Mode: 0, 1, 2, 3, 4 - UDMA Mode: 0, 1, 2, 3, 4, 5, 6, 7					
Average Access Time			0.3 ms(estimated)					
Maximum Performance	**Capacity**		2GB	4GB	8GB	16GB	32GB	64GB
	Sequential Read (MB/s)	**UDMA -6**	92.7	92.7	106.9	112.7	113.9	113.5
	Sequential Write(MB/s)	**UDMA -6**	39.7	70.0	71.2	66.5	83.8	83.8
The number of Channel			Qual.	Qual.	Qual.	Qual.	Qual.	Qual.

Note:

(1). All values quoted are typically at 25℃ and nominal supply voltage.

(2). Testing of the CompactFlash (CF) Card maximum performance was performed under the following platform:

- Computer with AMD 3.0GHz processor

- Windows XP Professional operating system

2.4. *System Reliability*

Table 4: System Reliability

Wear-leveling Algorithms	Global wear-leveling algorithms
ECC Technology	72 bits per 1024 bytes block

2.5. *Physical Specifications*

Refer to Table 5 and see Figure 2 for APRO industrial CompactFlash (CF) Card HERCULES-N Series physical specifications and dimensions.

Table 5: Physical Specifications

APRO industrial CompactFlash (CF) Card HERCULES-N Series	
Length:	36.40 ± 0.15 mm(1.433±0.006 in)
Width:	42.80 ± 0.10 mm(1.685±0.004 in)
Thickness:	3.3 mm ± 0.10 mm(0.130±0.004 in) (Excluding Lip)
Weight:	12 g (.40oz) typical, 15.0 g (.50 oz) maximum

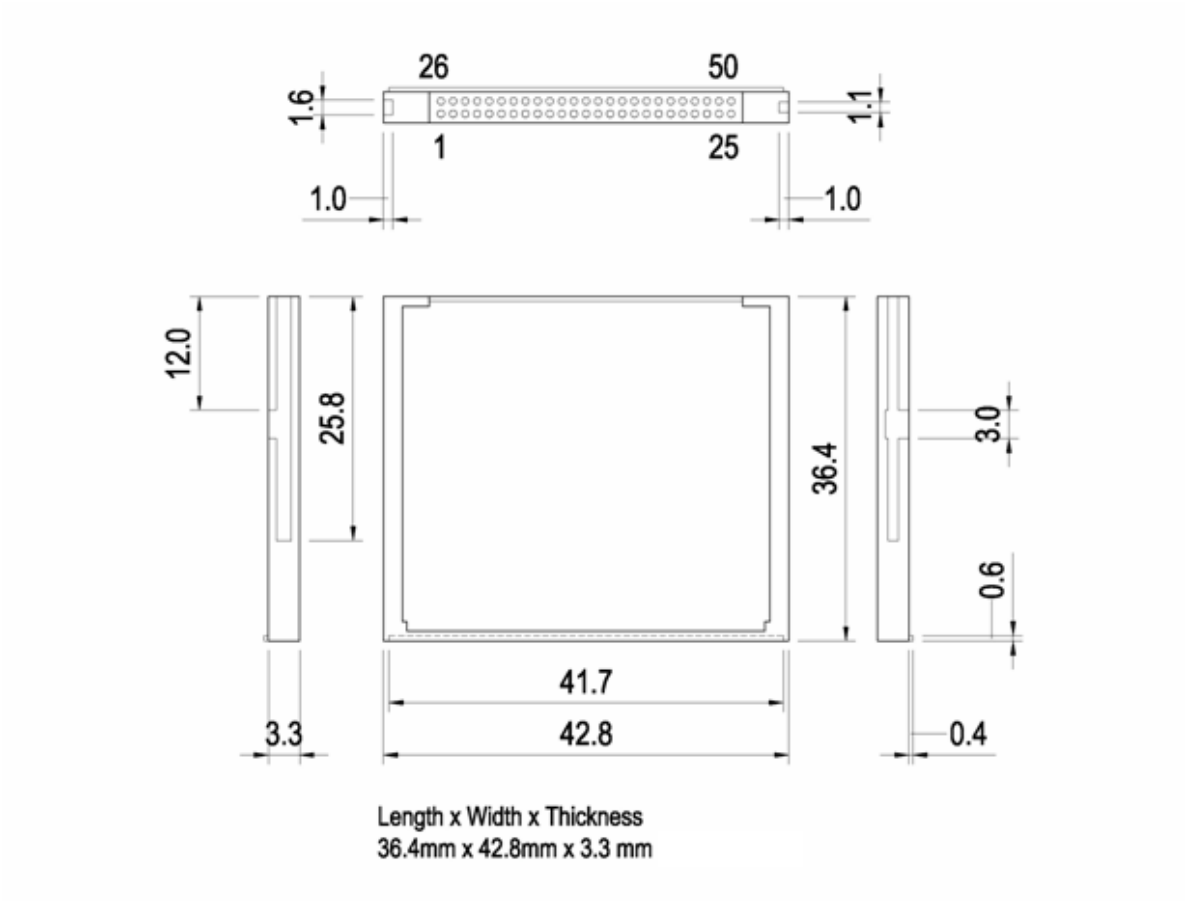

Figure 2: CompactFlash Card Dimension

2.6. *Device Parameter*

The table 6 shows the specific capacity for the various models and the default number of heads, sectors/track and cylinders.

Table 6: Device Parameter

Unformatted Capacity	Default Cylinder	Default Head	Default Sector	Default CHS Capacity
2GB	3,900	16	63	3,931,200
4GB	7,785	16	63	7,847,280
8GB	15,538	16	63	15,662,304
16GB	31,045	16	63	31,293,360
32GB	62,041	15	63	62,537,328
64GB	16,383	15	63	250,085,376

3. Interface Description

3.1. CF interface (CompactFlash Type I)

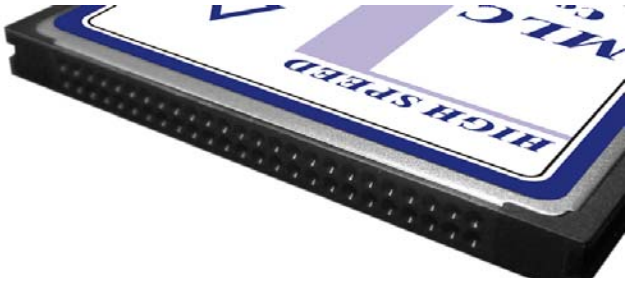

Figure 3: 50-pin CompactFlash Type I Connector

3.2. Pin Assignments

Signals whose source is the host is designated as inputs while signals that the CompactFlash (CF) Card sources are outputs. The pin assignments are listed in below table 7.

The signal/pin assignments are listed in below Table 7. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output.

Table 7: Pin Assignments and Pin Type

True IDE Mode[4]			
Pin Num	**Signal Name**	**Pin Type**	**In, Out Type**
1	GND		Ground
2	D03	I/O	11Z,OZ3
3	D04	I/O	11Z,OZ3
4	D05	I/O	11Z,OZ3
5	D06	I/O	11Z,OZ3
6	D07	I/O	11Z,OZ3
7	-CS0	I	13Z
8	A10[2]	GND	Ground
9	-ATA SEL	GND	Ground
10	A09[2]	GND	Ground
11	A08[2]	GND	Ground
12	A07[2]	GND	Ground
13	VCC		Power
14	A06[2]	GND	Ground
15	A05[2]	GND	Ground
16	A04[2]	GND	Ground
17	A03[2]	GND	Ground
18	A02	I	11Z

True IDE Mode[4]			
Pin Num	**Signal Name**	**Pin Type**	**In, Out Type**
19	A01	I	11Z
20	A00	I	11Z
21	D00	I/O	11Z,OZ3
22	D01	I/O	11Z,OZ3
23	D02	I/O	11Z,OZ3
24	-IOCS16	NC	ON3
25	-CD2	GND	Ground
26	-CD1	GND	Ground
27	D11[1]	I/O	11Z,OZ3
28	D12[1]	I/O	11Z,OZ3
29	D13[1]	I/O	11Z,OZ3
30	D14[1]	I/O	11Z,OZ3
31	D15[1]	I/O	11Z,OZ3
32	-CS1[1]	I	13Z
33	-VS1	GND	Ground
34	-IORD[7]	I	13Z
	HSTROBE[8]		
	-HDMARDY[9]		
35	-IOWR[7]	I	13Z
	STOP[8.9]		
36	-WE[3]	I	13U
37	INTRQ	O	OZ1
38	VCC		Power
39	-CSEL	I	12U
40	-VS2	NC	OPEN
41	-RESET	I	12Z
42	IORDY[7]	O	ON1
43	DMARQ	O	OZ1
44	-DMACK[6]	I	13U
45	-DASP	I/O	11U,ON1
46	-PDIAG	I/O	11U.ON1
47	D08[1]	I/O	11Z,OZ3
48	D09[1]	I/O	11Z,OZ3
49	D10[1]	I/O	11Z,OZ3

True IDE Mode[4]			
Pin Num	**Signal Name**	**Pin Type**	**In, Out Type**
50	GND		Ground

Note:

1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.

2) The signal should be grounded by the host.

3) The signal should be tied to VCC by the host.

4) The mode is optional for CF+ Cards, but required for CompactFlash Cards.

5) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.

6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition

7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.

8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.

9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.

3.3. *Electrical Description*

The CompactFlash Card HERCULES-N Series is optimized for operation with hosts, which support the PCMCIA/ I/O interface standard conforming to the PC Card ATA specification. However, the CompactFlash Card may also be configured to operate in systems that support only the memory interface standard. The configuration of the CompactFlash Card will be controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the CompactFlash Card.

Table 8: describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the CompactFlash Card sources are outputs. The CompactFlash Card logic levels conform to those specified in the *PCMCIA Release 2.1 Specification*. See Section 3.3 for definitions of Input and Output type.

Table 8: Signal Description

Signal Name	Dir	Pin	Description
A2 – A0 (True IDE Mode)	I	18,19,20	In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
-PDIAG (True IDE Mode)	I/O	46	In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
-DASP	I/O	45	In the True IDE Mode, this input/output is the Disk

Signal Name	Dir	Pin	Description
(True IDE Mode)			Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (True IDE Mode)	O	26,25	This signal is the same for all modes.
-CS0, -CS1 (True IDE Mode)	I	7,32	In the True IDE Mode, -CS0 is the chip select for the task file registers while –CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16bits.
-CSEL (True IDE Mode)	I	39	This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When the pin is open, this device is configured as a Slave.
D15 – D00 (True IDE Mode)	I/O	31,30,29,28 ,27,49,48,4 7,6,5,4,3,2, 23,22,21	In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (True IDE Mode)	--	1,50	This signal is the same for all modes.
DMARQ (True IDE Mode)	O	43	This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with –DMACK, i.e., the device shall wait until the host asserts –DMACK before negating DMARQ, and re-asserting DMARQ if there is more data to transfer. DMAARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device will not attempt

Signal Name	Dir	Pin	Description
			DMA mode. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.
-IORD (True IDE Mode –Except Ultra DMA Protocol Active) -HDMARDY (True IDE Mode – In Ultra DMA Protocol DMA Read) HSTROBE (True IDE Mode – In Ultra DMA Protocol DMA Write)	I	34	In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode. In True IDE Mode when Ultra DMA mode DMA Read is active this signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate –HDMARDY to pause an Ultra DMA transfer. In True IDE Mode when Ultra DMA mode DMA Write is active this signal is the data out strobe generated by the host. Both rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
-IOWR (True IDE Mode – Except Ultra DMA Protocol Active) STOP (True IDE Mode – Ultra DMA Protocol Active)	I	35	In True IDE Mode, while Ultra DMA mode protocol is not active this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol. In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
-ATA SEL (True IDE Mode)	I	9	To enable True IDE Mode this input should be grounded by the host.
INTRQ (True IDE Mode)	O	37	In True IDE Mode signal is the active high Interrupt Request to the host.
-DMACK (True IDE Mode)	I	44	This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the –DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC

Signal Name	Dir	Pin	Description
			by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
-RESET (True IDE Mode)	I	41	In the True IDE Mode, this input pin is the active low hardware reset from the host.
VCC (True IDE Mode)	--	13,38	This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)	O	33 40	This signal is the same for all modes.
IORDY (True IDE Mode –Except Ultra DMA Mode) -DDMARDY (True IDE Mode –Ultra DMA Write Mode) DSTROBE (True IDE Mode –Ultra DMA Read Mode)	O	42	In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate –DDMARDY to pause an Ultra DMA transfer. In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
-WE (PC Card Memory Mode) -WE (PC Card I/O Mode) -WE (True IDE Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
-IOIS16	O	24	In True IDE Mode this output signal is asserted low when this

Signal Name	Dir	Pin	Description
(True IDE Mode)			device is expecting a word data transfer cycle.

3.4. *Electrical Specification*

Table 9, Table 10, and Table 11 defines all D.C. Characteristics for the CompactFlash (CF) Card. Unless otherwise stated, electrical condition is as below Table 9:

Table 9: Electrical Condition

Commercial Grade **SPCFCxxxG-MNCTC** **SRCFCxxxG-MNCTC**	**Industrial Grade** **WPCFCxxxG-MNITI** **WRCFCxxxG-MNITI**
Vcc = 5V ±10% Vcc = 3.3V ± 5% Ta = 0°C to +70°C	Vcc = 5V ±10% Vcc = 3.3V ± 5% Ta = -40°C to +85°C

3.5. *General DC Characteristics*

3.5.1. Interface I/O at 5.0V

Table 10: Interface I/O at 5.0V

Symbol	Parameter	Min.	Max.	Units	Remark
V_{CC}	Power Supply	4.5	5.5	V	
V_{OH}	Output Voltage High Level	2.5		V	
V_{OL}	Output Voltage Low Level		0.4	V	
V_{IH}	Input Voltage High Level	2.4		V	Non-schmitt trigger
		2.05		V	Schmitt trigger[1]
V_{IL}	Input Voltage Low Level		0.6	V	Non-schmitt trigger
			1.25	V	Schmitt trigger[1]
R_{PU}	Pull up resistance[2]	52.7	141	kOhm	
R_{PD}	Pull down resistance	47.5	172	kOhm	

3.5.2. Interface I/O at 3.3V

Table 11: Interface I/O at 3.3V

Symbol	Parameter	Min.	Max.	Units	Remark
VCC3H	Power Supply	2. 7	3.6	V	
VCC3F					
V_{OH}	Output Voltage High Level	0.9 x V_{IO}		V	
V_{OL}	Output Voltage Low Level		0.1 x V_{IO}	V	
V_{IL}	Input Voltage High Level	1.51	1.75	V	Non-schmitt trigger

		1.61	1.84	V	Schmitt trigger[1]
V_{CC}	Input Voltage Low Level	1.51	1.74	V	Non-schmitt trigger
		1.38	1.61	V	Schmitt trigger[1]
R_{PU}	Pull up resistance2	52.7	141	kOhm	
R_{PD}	Pull down resistance	47.5	172	kOhm	

Notes:

1) Include CE1, CE2, HREG, HOE, HIOE, HWE, HIOW pins.

2) Include CE1, CE2, HREG, HOE, HIOE, HWE, HIOW, CSEL, PDIAG, DASP pins.

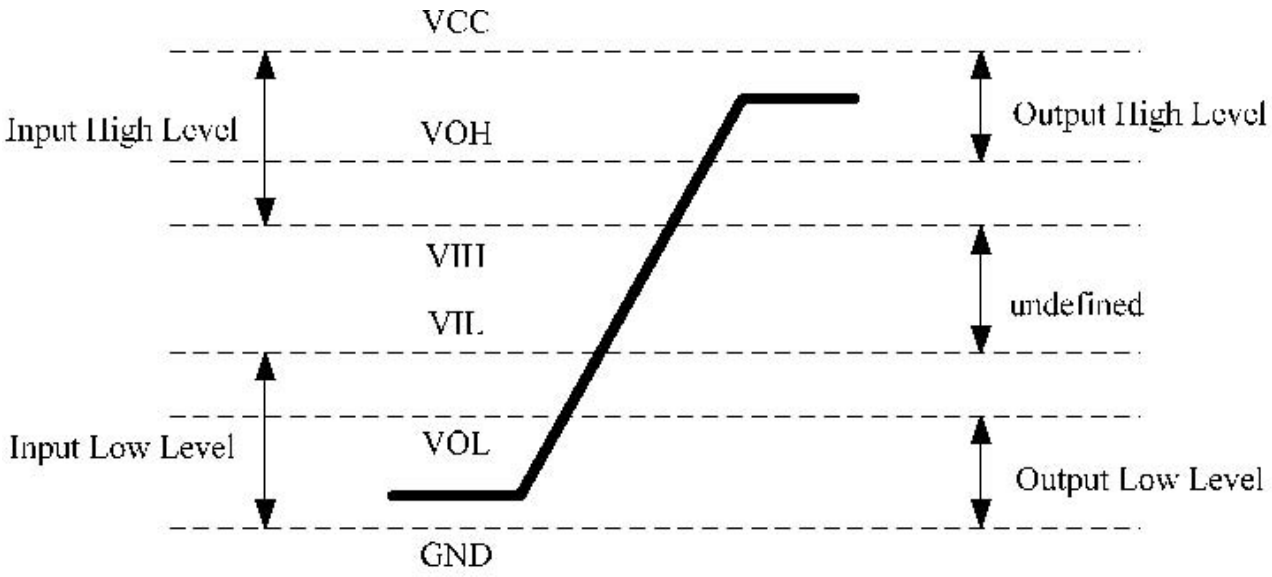

Figure 4: Interface I/O Voltage Diagram

3.6. *AC Characteristics*

3.6.1. Attribute Memory Read Timing

Table 12: Attribute Memory Read Timing

Speed Version	**Symbol**	**300 ns**	
Item		**Min ns.**	**Max ns.**
Read Cycle Time	tc(R)	300	
Address Access Time	ta (HA)		300
Card Enable Access Time	ta (CEx)		300
Output Enable Access Time	ta (HOE)		150
Output Disable Time from CEx	tdis (CEx)		100
Output Disable Time from HOE	tdis (HOE)		100
Address Setup Time	tsu (HA)	30	
Output Enable Time from CEx	ten (CEx)	5	
Output Enable Time from HOE	ten (HOE)	5	

Data Valid from Address Change	tv(HA)	0	

Notes:

All time intervals are recorded in nanoseconds. HD refers to data provided by the CompactFlash Card to the system. The CEx# signal or both the HOE# signal and the HWE# signal are deasserted between consecutive cycle operations.

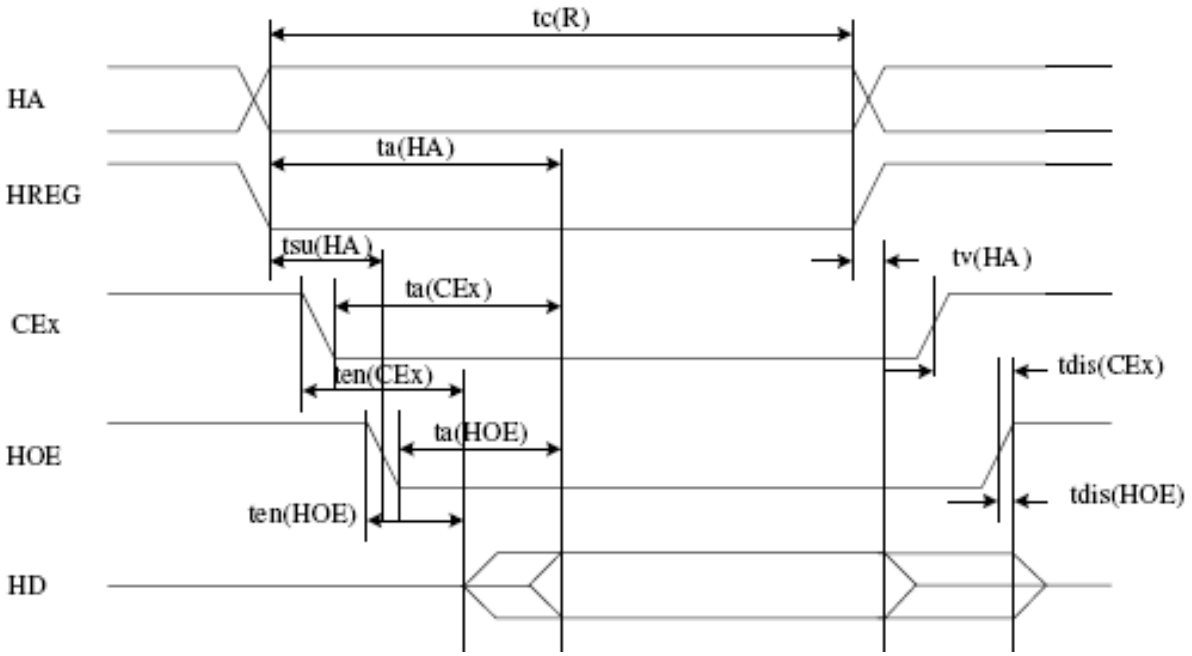

Figure 5: Attribute Memory Read Timing Diagram

3.6.2. Configuration Register (Attribute Memory) Write Time

Table 13: Configuration Register (Attribute Memory) Write Time

Speed Version	**Symbol**	**250 ns**	
Item		**Min ns.**	**Max ns.**
Write Cycle Time	tc(W)	250	
Write Pulse Width	tw (HWE)	150	
Address Setup Time	tsu (HA)	30	
Write Recovery Time	trec (HWE)	30	
Data Setup Time for HWE	tsu (HD-HWEH)	80	
Data Hold Time	th (HD)	30	

Notes: All times are in nanoseconds. HD signifies data provided by the system to the CompactFlash (CF) Card.

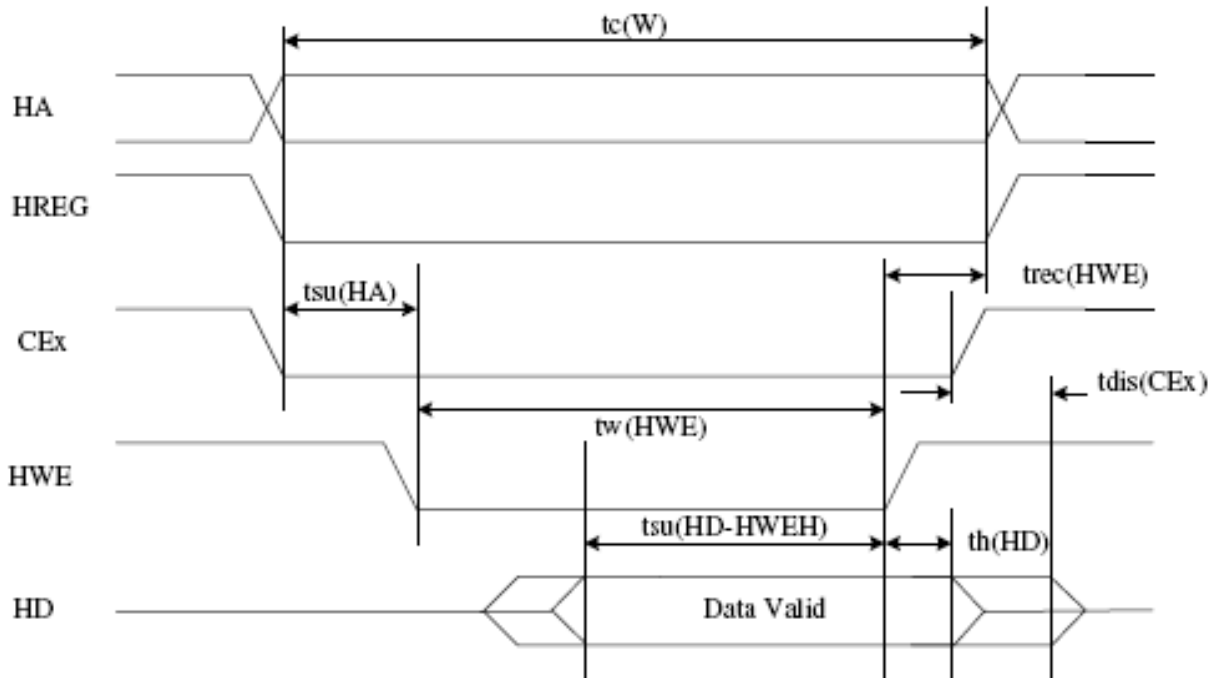

Figure 6: Configuration Register (Attribute Memory) Write Timing Diagram

3.6.3. Common Memory Read Timing

Table 14: Common Memory Reading Timing

Cycle Time Mode		**250 ns**		**120 ns**		**100 ns**		**80 ns**	
Item	**Symbol**	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Output Enable Access Time	ta (HOE)		125		60		50		45
Output Disable Time from	tdis (HOE)		100		60		50		45
Address Setup Time	tsu (HA)	30		15		10		10	
Address Hold Time	th (HA)	20		15		15		10	
CEx Setup before HOE	tsu (CEx)	0		0		0		0	
CEx Hold following HOE	th (CEx)	20		15		15		10	
Wait Delay Falling from HOE	tv (IORDY-HOE)		35		35		35		Na[1]
Data Setup for Wait Release	tv(IORDY)		0		0		0		Na[1]
Wait Width Time [2]	tw(IORDY)		350		350		350		Na[1]

Notes:

1) IORDY is not supported in this mode

2) The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. HD refers to data provided by the CompactFlash Card to the system. The IORDY signal can be

ignored when the HOE# cycle-to-cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure (CIS). Although adhering to the PCMCIA specification of 12 µs, the Wait Width time is intentionally lower in this specification.

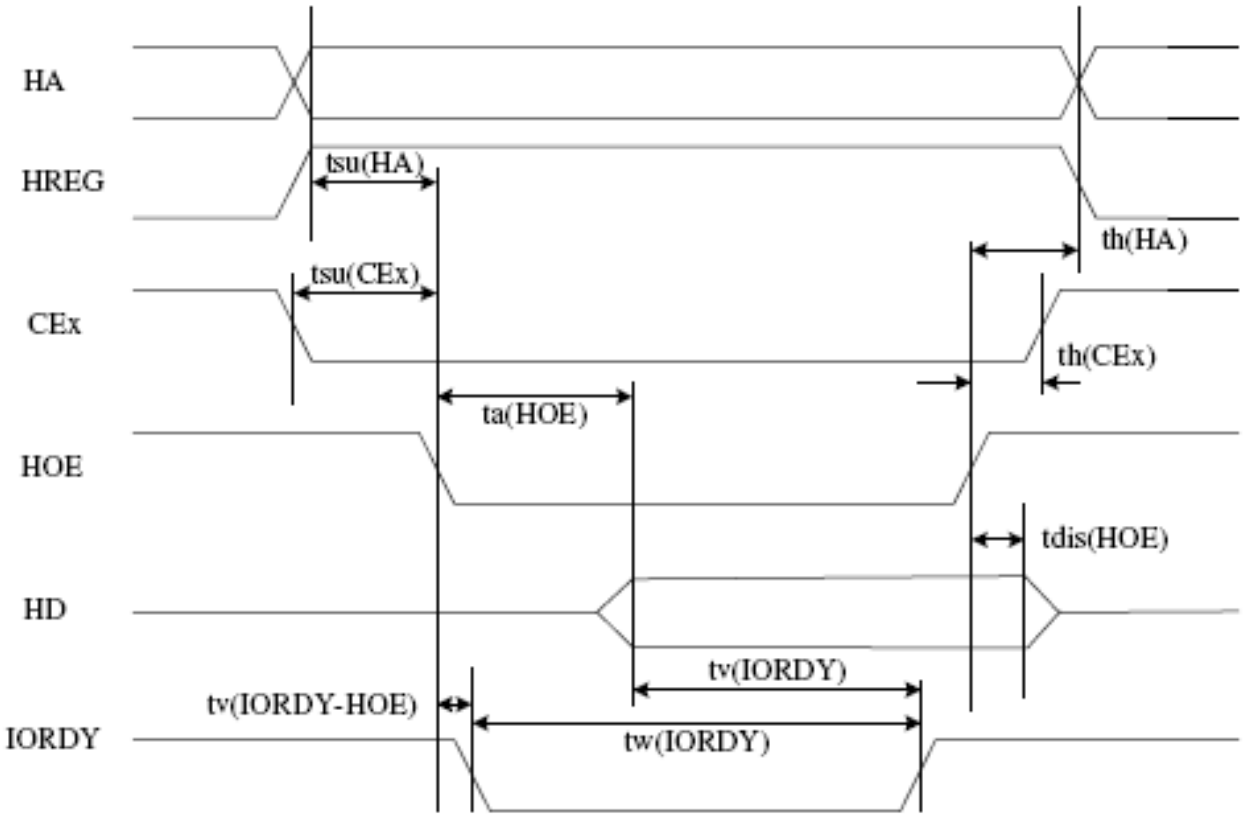

Figure 7: Common Memory Read Timing Diagram

3.6.4. Common Memory Write Timing

Table 14: Common Memory Write Timing

Cycle Time Mode		**250 ns**		**120 ns**		**100 ns**		**80 ns**	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before HWE#	tsu(HD-HWEH)	80		50		40		30	
Data Hold following HWE#	th(HD)	30		15		10		10	
HWE# Pulse Width	tw(HWE)	150		70		60		55	
Address Setup Time	tsu(HA)	30		15		10		10	
Address Hold Time	tsu(CEx)	0		0		0		0	
CEx# Setup before HWE#	trec(HWE)	30		15		15		15	
Write Recovery Time	th(HA)	20		15		15		15	
Address Hold Time	th(CEx)	20		15		15		10	

CEx# Hold following HWE#	tv(IORDY-HWE)		35				35		na[1]
Wait Delay Falling from HWE#	tv(IORDY)	0		0		0		na[1]	
HWE# High from Wait Release	tw (IORDY)		350				350		na[1]

Notes:

1) *IORDY is not supported in this mode.*

2) *The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec Cycle Time) total load. All time intervals are recorded in nanoseconds. HD refers to data provided by the CompactFlash Card to the system. The IORDY signal can be ignored when the HWE# cycle-to-cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure (CIS). Although adhering to the PCMCIA specification of 12 µs, the Wait Width time is intentionally lower in this specification.*

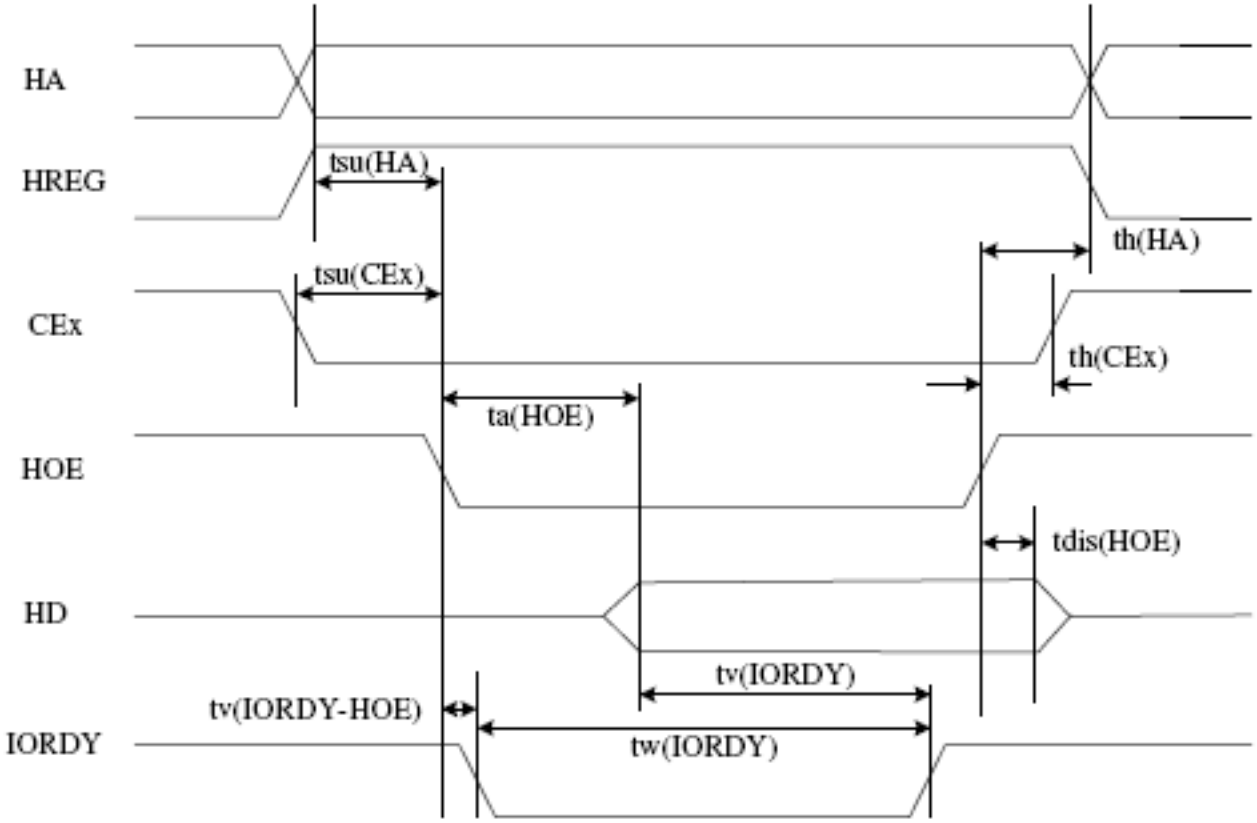

Figure 7: Common Memory Read Timing Diagram

3.6.5. I/O Read Timing

Table 15: I/O Read Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Delay after HIOE	td (HIOE)		100		50		50		45

Data Hold following HIOE	th (HIOE)	0		5		5		5	
HIOE Width Time	tw (HIOE)	165		70		65		55	
Address Setup before HIOE	tsuHA (HIOE)	70		25		25		15	
Address Hold following HIOE	tsuHA (HIOE)	20		10		10		10	
CEx Setup before HIOE	tsuCEx (HIOE)	5		5		5		5	
CEx Hold following HIOE	thCEx (HIOE)	20		10		10		10	
HREG Setup before HIOE	tsuHREG(HIOE)	5		5		5		5	
HREG Hold following HIOE	thHREG (HIOE)	0		0		0		0	
Wait Delay Falling from HIOE[2]	tdIORDY(HIOE)		35		35		35		na[1]
Data Delay from Wait Rising[2]	td(IORDY)		0		0		0		na[1]
Wait Width Time [2]	tw(IORDY)		350		350		350		na[1]

Notes:

1) *IORDY is not supported in this mode*

2) *Maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met. HD refers to data provided by the CompactFlash Card to the system. Although adhering to the PCMCIA specification of 12 µs, the Wait Width time is intentionally lower in this specification*

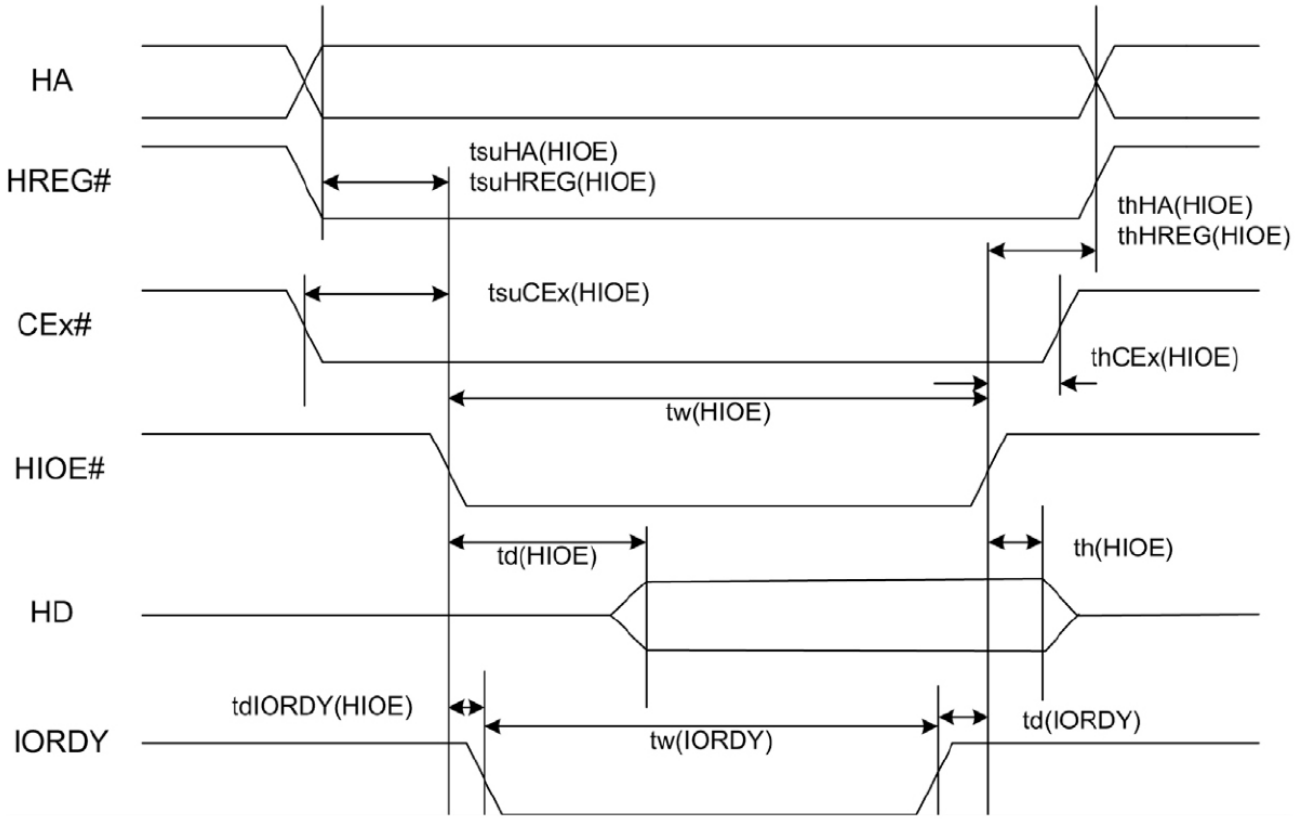

Figure 8: I/O Read Timing Diagram

3.6.6. I/O Write Timing

Table 16: I/O Write Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before HIOW	tsu (HIOW)	60		20		20		15	
Data Hold following HIOW	th (HIOW)	30		10		5		5	
HIOW Width Time	tw (HIOW)	165		70		65		55	
Address Setup before HIOW	tsuHA (HIOW)	70		25		25		15	
Address Hold following HIOW	tsuHA (HIOW)	20		20		10		10	
CEx Setup before HIOW	tsuCEx (HIOW)	5		5		5		5	
CEx Hold following HIOW	thCEx (HIOW)	20		20		10		10	
HREG Setup before HIOW	tsuHREG(HIOW)	5		5		5		5	
HREG Hold following HIOW	thHREG (HIOW)	0		0		0		0	
Wait Delay Falling from HIOW[2]	tdlORDY(HIOW)		35		35		35		na[1]
HIOW High from Wait High [2]	tdrHIOW(IORDY)	0		0		0		na[1]	
Wait Width Time [2]	tw(IORDY)		350		350		350		Na[1]

Notes:

1) *IORDY is not supported in this mode*

2) *The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. Although minimum time from IORDY high to HIOW# high is 0 nsec, the minimum HIOW# width is still met. HD refers to data provided by the CompactFlash Card to the system. Although adhering to the PCMCIA specification of 12 µs, the Wait Width time is intentionally lower in this specification*

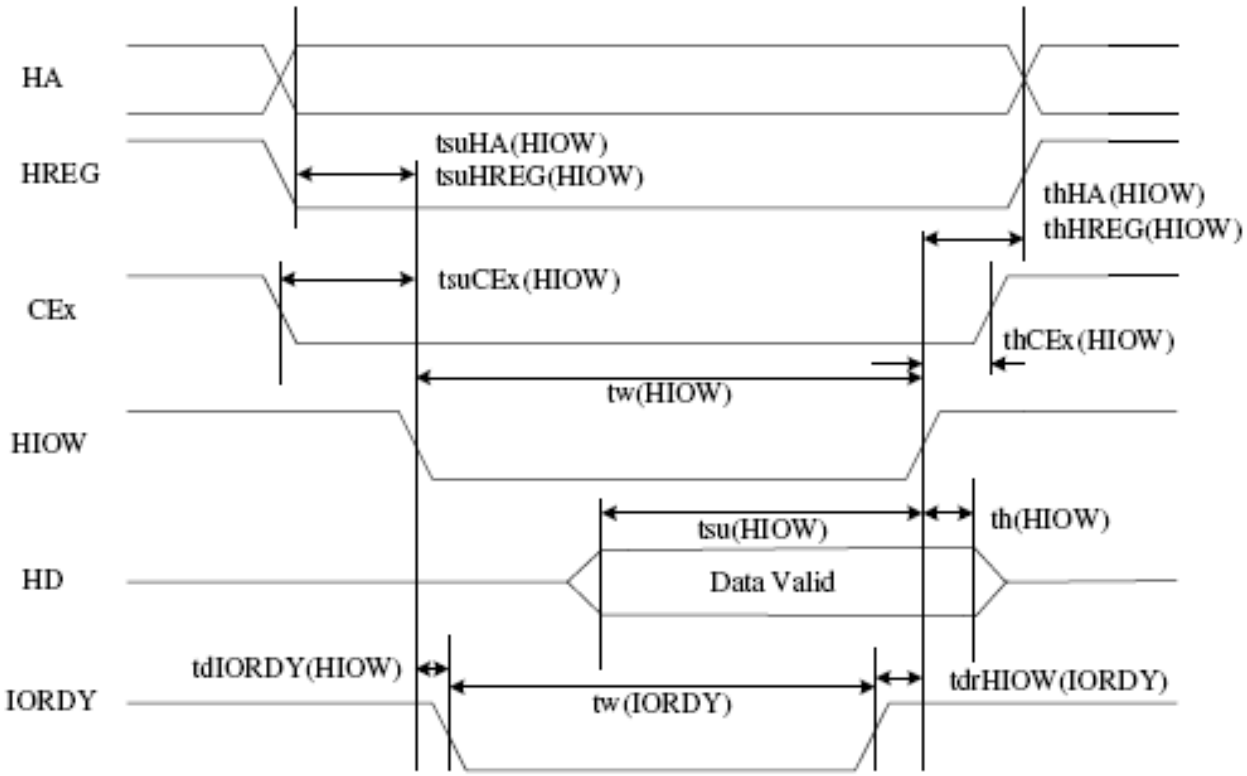

Figure 9: I/O Write Timing Diagram

3.6.7. True IDE PIO Mode Read/Write Timing

Table 17: True IDE PIO Mode Read/Write Timing

Item		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
t0	Cycle time (min)1	600	383	240	180	120	100	80
t1	Address Valid to HIOE/HIOW setup (min)	70	50	30	30	25	15	10
t2	HIOE/HIOW (min)1	165	125	100	80	70	65	55
t2	HIOE/HIOW (min) Register (8 bit)1	290	290	290	80	70	65	55
t2i	HIOE/HIOW recovery time (min)1	-	-	-	70	25	25	20
t3	HIOW data setup (min)	60	45	30	30	20	20	15
t4	HIOW data hold (min)	30	20	15	10	10	5	5
t5	HIOE data setup (min)	50	35	20	20	20	15	10
t6	HIOE data hold (min)	5	5	5	5	5	5	5
t6Z	HIOE data tristate (max)2	30	30	30	30	30	20	20
t7	Address valid to IOCS16 assertion (max)4	90	50	40	n/a	n/a	n/a	n/a
t8	Address valid to IOCS16 released (max)4	60	45	30	n/a	n/a	n/a	n/a
t9	HIOE/HIOW to address valid hold	20	15	10	10	10	10	10

tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0
tA	IORDY Setup time3	35	35	35	35	35	na[5]	na[5]
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na[5]	na[5]
tC	IORDY assertion to release (max)	5	5	5	5	5	na[5]	na[5]

Notes:

All timings are in nanoseconds. The maximum load on IOCS16# is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met.

1) *Where t0 denotes the minimum total cycle time; t2 represents the minimum command active time; t2i is the minimum command recovery time or command inactive time. Actual cycle time equals the sum of actual command active time and actual command inactive time. The three timing requirements for t0, t2, and t2i are met. The minimum total cycle time requirement is greater than the sum of t2 and t2i, implying that a host implementation can extend either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identity data. A CompactFlash Card implementation supports any legal host implementation.*
2) *This parameter specifies the time from the negation edge of the HIOE# to the time that the CompactFlash Card (tri-state) no longer drives the data bus.*
3) *The delay originates from HIOE# or HIOW# activation until the state of IORDY is first sampled. If IORDY is inactive, the host waits until IORDY is active before the PIO cycle is completed. When the CompactFlash Storage Card is not driving IORDY, which is negated at tA after HIOE# or HIOW# activation, then t5 is met and tRD is inapplicable. When the CompactFlash Card is driving IORDY, which is negated at the time tA after HIOE# or HIOW# activation, then tRD is met and t5 is inapplicable.*
4) *Both t7 and t8 apply to modes 0, 1, and 2 only. For other modes, this signal is invalid.*
5) *IORDY is not supported in this mode.*

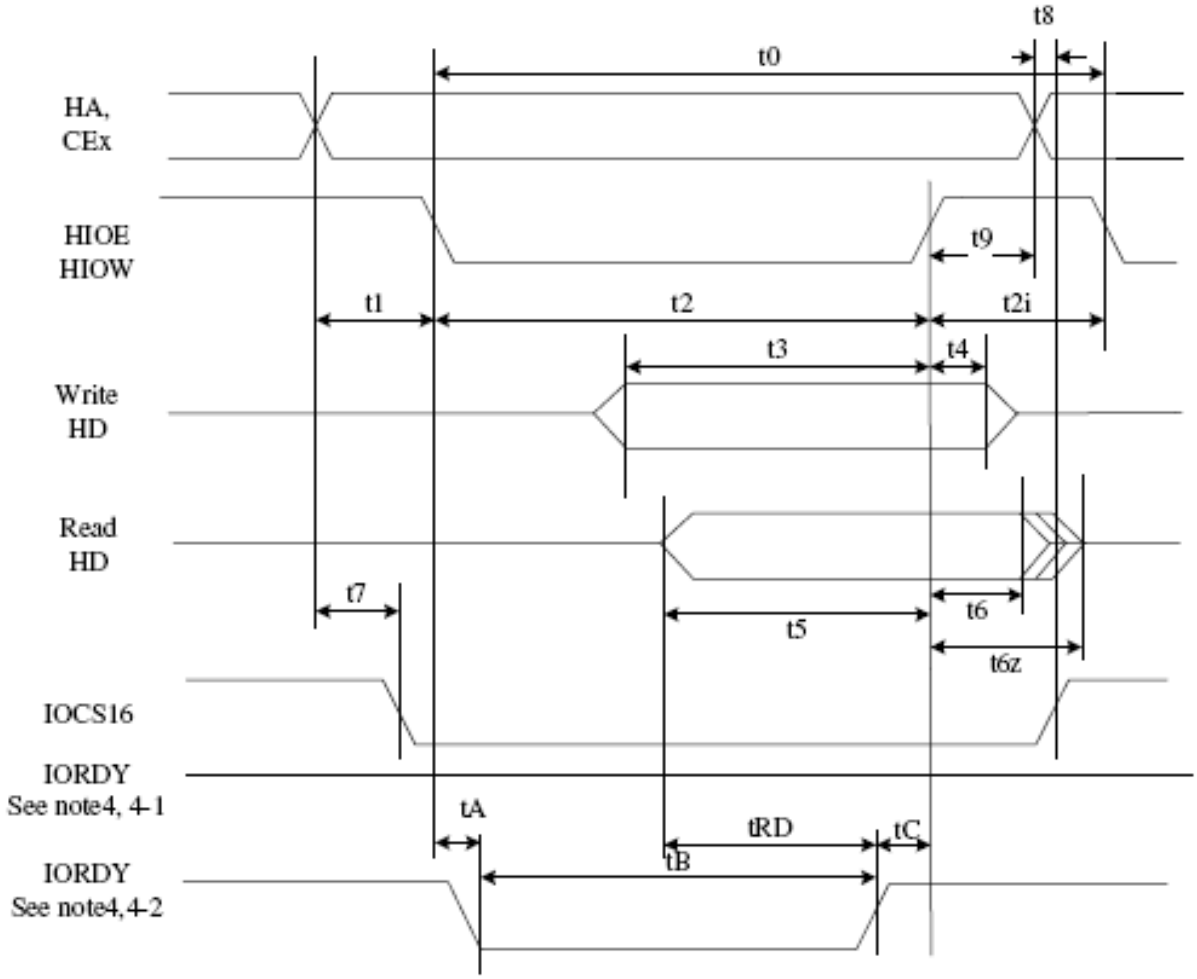

Figure 10: True IDE PIO Mode Read/Write Timing Diagram

Notes:

1) *Device address comprises CE1#, CE2#, and HA[2:0].*
2) *Data comprises HD[15:0] (16-bit) or HD[7:0] (8-bit).*
3) *IOCS16# is shown for PIO modes 0, 1, and 2. For other modes, this signal is ignored.*
4) *The negation of IORDY by the device is used to lengthen the PIO cycle. Whether the cycle is to be extended is determined by the host after tA from the assertion of HIOE# or HIOW#. The assertion and negation of IORDY is described in the following three cases.*
   (a) *The device never negates IORDY: No wait is generated.*
   (b) *Device drives IORDY low before tA: a wait is generated. The cycle is completed after IORDY is reasserted. For cycles in which a wait is generated and HIOE# is asserted, the device places read data on D15-D00 for tRD before IORDY is asserted.*

3.6.8. True IDE Multiword DMA Mode Read/Write Timing

Table 18: True IDE Multiword DMA Mode Read/Write Timing

Item		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note
tO	Cycle time (min)	480	150	120	100	80	1
tD	HIOE / HIOW asserted width (min)	215	80	70	65	55	1
tE	HIOE data access (max)	150	60	50	50	45	
tF	HIOE data hold (min)	5	5	5	5	5	
tG	HIOE/HIOW data setup (min)	100	30	20	15	10	
tH	HIOW data hold (min)	20	15	10	5	5	
tI	DMACK(HREG) to HIOE/HIOW setup (min)	0	0	0	0	0	
tJ	HIOE / HIOW to -DMACK hold (min)	20	5	5	5	5	
tKR	HIOE negated width (min)	50	50	25	25	20	1
tKW	HIOW negated width (min)	215	50	25	25	20	1
tLR	HIOE to DMARQ delay (max)	120	40	35	35	35	
tLW	HIOW to DMARQ delay (max)	40	40	35	35	35	
tM	CEx valid to HIOE / HIOW	50	30	25	10	5	
tN	CEx hold	15	10	10	10	10	

Notes:

1) Where t0 is the minimum total cycle time and tD is minimum command active time, whereas tKR and tKW are minimum command recovery time or command inactive time for input and output cycles, respectively. Actual cycle time equals the sum of actual command active time and actual command inactive time. The three timing requirements of t0, i.e. tD, tKR, and tKW, must be met. The minimum total cycle time requirement exceeds the sum of tD and tKR or tKW for input and output cycles, respectively, implying that a host implementation can extend either or both tD and tKR or tKW as deemed necessary to ensure that t0 equals or exceeds the value reported in the device's identity data. A CompactFlash Card implementation supports any legal host implementation.

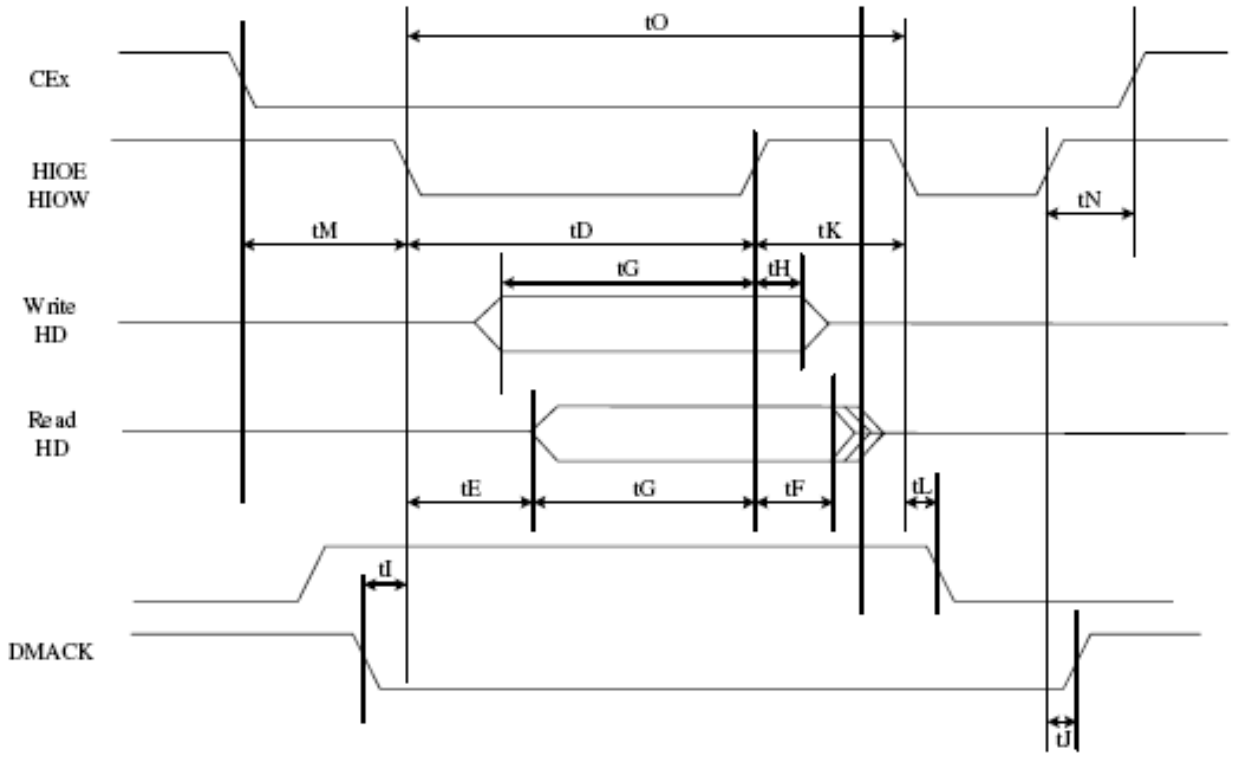

Figure 11: True IDE Multiword DMA Mode Read/Write Timing Diagram

Notes:

1) *If a card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ during the time from the start of a DMA transfer cycle (to suspend DMA transfers in progress) and reassertion of the signal at a relatively later time to continue DMA transfer operations.*
2) *The host may negate this signal to suspend the DMA transfer in progress.*

3.6.9. Ultra DMA Signal in Each Interface Mode

Table 19: Ultra DMA Signal in True IDE Mode

Signal	Type	(Non UDMA Memory Mode)	PC Card Memory Mode UDMA	PC Card IO Mode UDMA	TRUE IDE MODE UDMA
DMARQ	Output	(-INPACK)	-DMARQ	-DMARQ	DMARQ
HREG	Input	(-REG)	- DMARQ	DMARQ	- DMARQ
HIOW	Input	(-IOWR)	STOP[1]	STOP[1]	STOP[1]
HIOE	Input	(-IORD)	-HDMARDY(R)[1,2] HSTROBE(W)[1,3,4]	-HDMARDY(R)[1,2] HSTROBE(W)[1,3,4]	-HDMARDY(R)[1,2] HSTROBE(W)[1,3,4]
IORDY	Output	(-WAIT)	-DDMARDY(W)[1,3] DSTROBE(R)[1,2,4]	-DDMARDY(W)[1,3] DSTROBE(R)[1,2,4]	-DDMARDY(W)[1,3] DSTROBE(R)[1,2,4]
HD〔15:00〕	Bidir	(D〔15:00〕)	D〔15:00〕	D〔15:00〕	D〔15:00〕
HA〔10:00〕	Input	(A〔10:00〕)	A〔10:00〕[5]	A〔10:00〕[5]	A〔02:00〕[5]

CSEL	Input	(-CSEL)	-CSEL	-CSEL	-CSEL
HIRQ	Output	(READY)	READY	-INTRQ	INTRQ
CE1	Input	(-CE1)	-CE1	-CE1	-CS0
CE2		(-CE2)	-CE2	-CE2	-CS1

Notes:

1) *The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.*
2) *The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Read command.*
3) *The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.*
4) *The HSTROBE signals are active on both the rising and the falling edge.*
5) *Address lines 03 through 10 are not used in True IDE mode.*

3.6.10. Ultra DMA Data Burst Timing Requirement

Table 20: Ultra DMA Data Burst Timing Requirement

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		UDMA Mode 5		UDMA Mode 6		UDMA Mode 7		Measure Location
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	(See Note 2)
$t_{2CYCTYP}$	240		160		120		90		60		40		30		24		Sender
t_{CYC}	112		73		54		39		25		16.8		13.0		10		Note3
t_{2CYC}	230		153		115		86		57		38		29		23		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		2.6		2.5		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		3.5		2.9		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		4.0		2.9		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		4.0		3.2		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		10.0		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		10.0		10.0		Host
t_{ZFS}	0		0		0		0		0		35		25		15.0		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		17.5		10.5		Sender
t_{FS}		230		200		170		130		120		90		80		70	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	0	60	0	50	Note4
t_{MLI}	20		20		20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10		10		10	Note5
t_{ZAH}	20		20		20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		0		0		Device

t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	20	50	20	50	Host
t_{RFS}		75		70		60		60		60		50		50		50	Sender
t_{RP}	160		125		100		100		100		85		85		85		Recipient
t_{IORDYZ}		20		20		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		25		25		25		Sender

Notes: All Timings in ns

1) *All timing measurement switching points (low to high and high to low) are taken at 1.5V.*
2) *All signal transitions for a timing parameter are determined at the connector specified in the measurement location column. For instance, for the case of tRFS, both STROBE and DMARDY# transitions are determined by the sender's connector.*
3) *Parameter tCYC is determined at the connector of the recipient farthest from the sender.*
4) *Parameter tLI is determined at the connector of a sender or recipient responding to an incoming transition from the recipient or sender, respectively. Both incoming signal and outgoing response are determined at the same connector.*
5) *Parameter tAZ is determined at the connector of a sender or recipient driving the bus, and must release the bus to allow for a bus turnaround.*
6) *Table 25 lists the AC Timing requirements: Ultra DMA AC Signal Requirements*

3.6.11. Ultra DMA Data Burst Timing Descriptions

Table 21: Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2,5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2,5
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	

t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	6
t_{ZIORDY}	Minimum time before driving IORDY	4,6
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

1) *Parameters tUI, tMLI (in Figure 16: Ultra DMA Data-In Burst Device Termination Timing and Figure 17: Ultra DMA Data-In Burst Host Termination Timing), and tLI represent sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (sender or recipient) is waiting for the other agent to respond with a signal before proceeding. Parameter tUI denotes an unlimited interlock that has no maximum time value; tMLI represents a limited time-out that has a defined minimum; tLI is a limited time-out that has a defined maximum.*
2) *The 80-conductor cabling is required to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes exceeding 2.*
3) *Timing for tDVS, tDVH, tCVS, and tCVH must be met for lumped capacitive loads of 15 and 40 pF at the connector where the data and STROBE signals have the same capacitive load value. Due to cable reflections, these timing measurements are invalid in a system functioning normally.*
4) *For all timing modes, parameter tZIORDY may be greater than tENV since the host has a pull-up on IORDY giving it a known state when released.*
5) *Parameters tDS and tDH for mode 5 are defined for a recipient at the end of a cable only in a configuration that has a single device located at the cable end. This configuration can result in tDS and tDH for mode 5 at the middle connector having minimum values of 3.0 and 3.9 ns, respectively.*
6) *The parameters are applied to True IDE mode operation only.*

3.6.12. Ultra DMA Sender and Recipient IC Timing Requirements

Table 22: Ultra DMA Sender and Recipient IC Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		UDMA Mode 5		UDMA Mode 6		UDMA Mode 7	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	14.7		9.7		6.8		6.8		4.8		2.2		2.3		2.3	
t_{DHIC}	4.8		4.8		4.8		4.8		4.8		2.8		2.8		2.8	
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5		6.0		5.2		3.7	
t_{DVHIC}	9.0		9.0		9.0		9.0		9.0		6.0		5.2		3.7	
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)															
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)															
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)															
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)															

Notes:

1) *All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.*
2) *The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V).*
3) *The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.*

3.6.13. Ultra DMA AC Signal Requirements

Table 23: Ultra DMA AC Signal Requirements

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
SRISE	Rising Edge Slew Rate for any signal		1.25	1
SFALL	Falling Edge Slew Rate for any signal		1.25	1

Notes:

1) *The sender is tested while driving an 18 inch, 80 conductor cable with PVC insulation. The signal being tested must be cut at a test point such that it has no trace, cable, or recipient loading after the test point. All other signals must remain connected through to the recipient. The test point should be located between a sender's series termination resistor and within 0.5 inch or less from where the conductor exits the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor must also be cut within 0.5 inch of the connector.*

   The test load and test points should be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or relatively smaller capacitor connected between the test point and ground. Slew rates are met for both capacitor values.

   Measurements must be taken at the test point using a <1 pF, >100 kΩ, 1 Ghz probe and a 500 MHz oscilloscope. The average rate is measured from 20-80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level

must be measured as the average high output level under the defined test conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge..

3.6.14. Ultra DMA Data-In Burst Initiation Timing

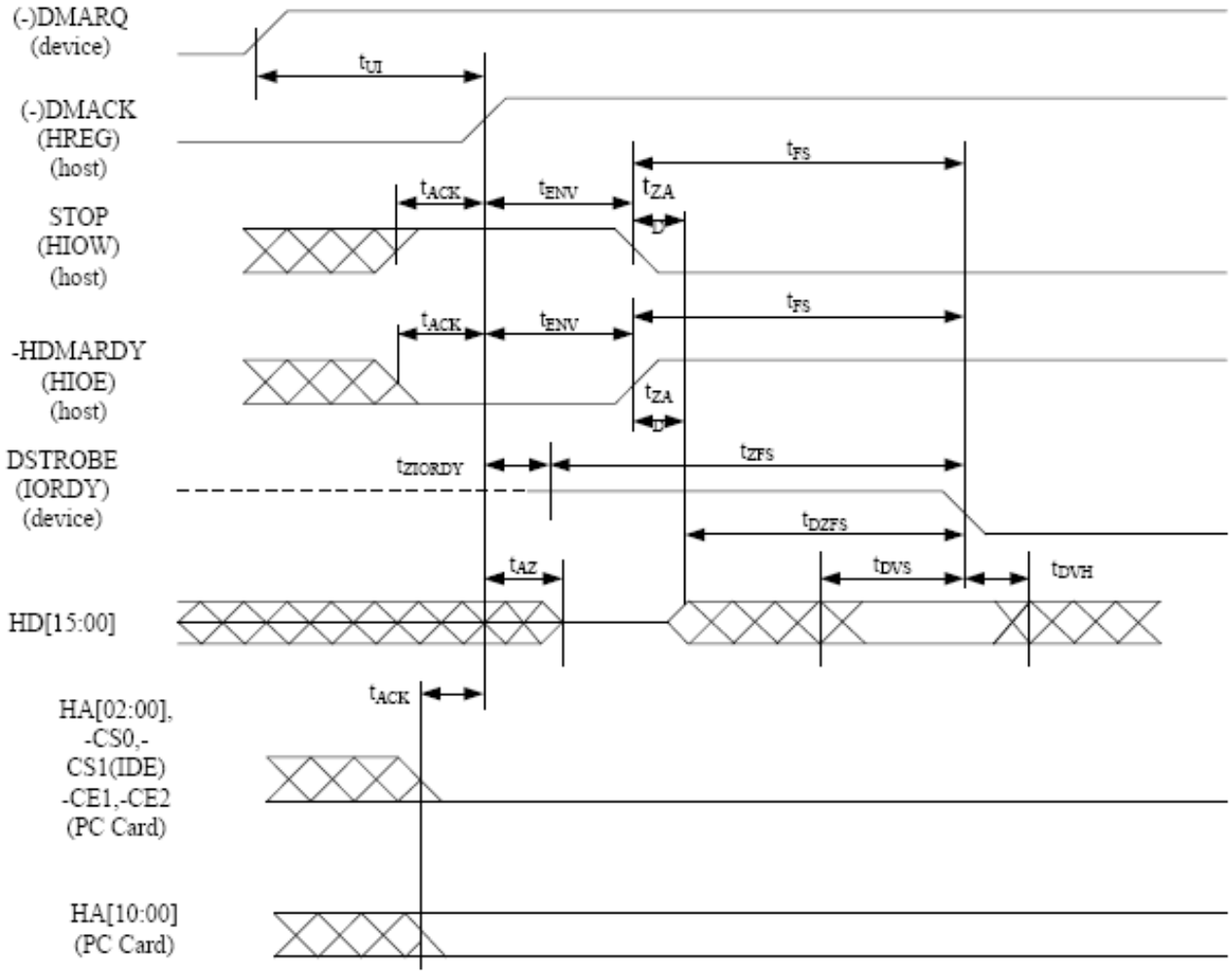

Figure 12: Ultra DMA Data-in Burst Initiation Timing Diagram

Notes:

1) *All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.*
2) *The definitions for the IORDY:DDMARDY#:DSTROBE, HIOE#: HDMARDY#: HSTROBE and HIOW#: STOP signal lines are not in effect until DMARQ(#) and DMACK(#) are asserted. Notably, HA[2:0], CS0# and CS1# are True IDE mode signal definitions, and HA[10:0], CE1# and CE2# are PC Card mode signals. The Bus polarity of DMACK(#) and DMARQ(#) is based on the active interface mode.*

3.6.15. Sustained Ultra DMA Data-In Burst Timing

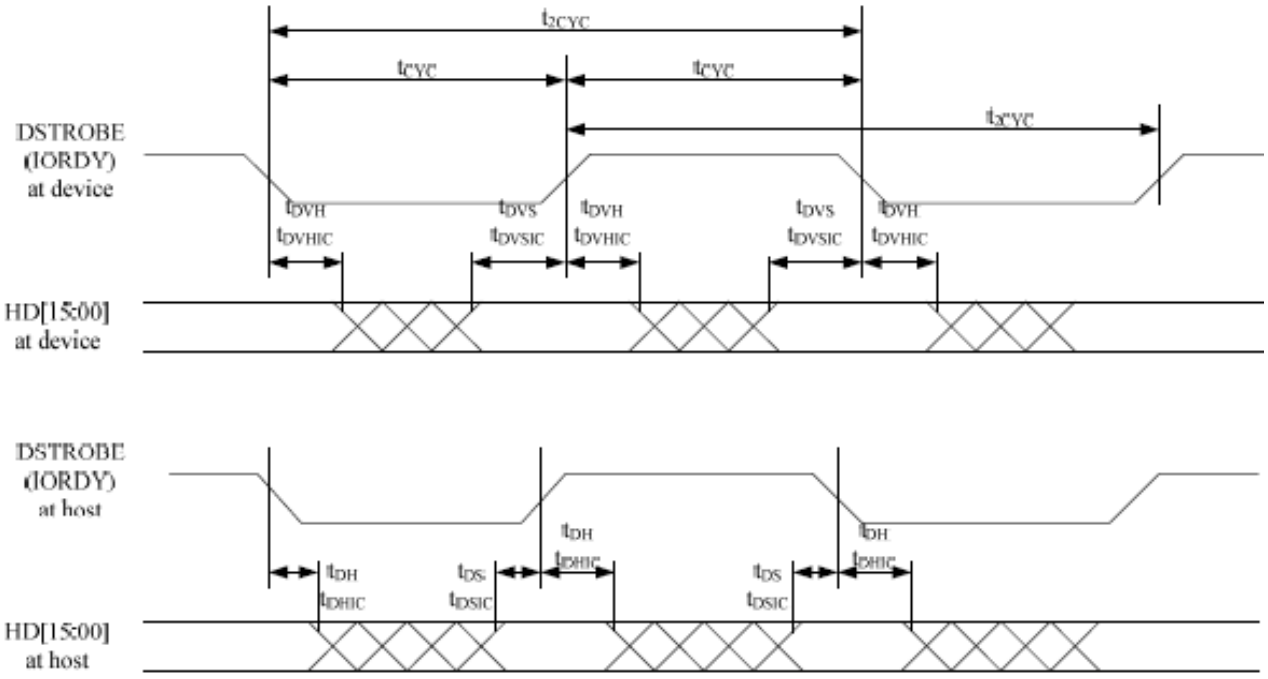

Figure 13: Sustained Ultra DMA Data-in Burst Initiation Timing Diagram

Note:

HD [15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

3.6.16. Ultra DMA Data-In Burst Host Pause Timing

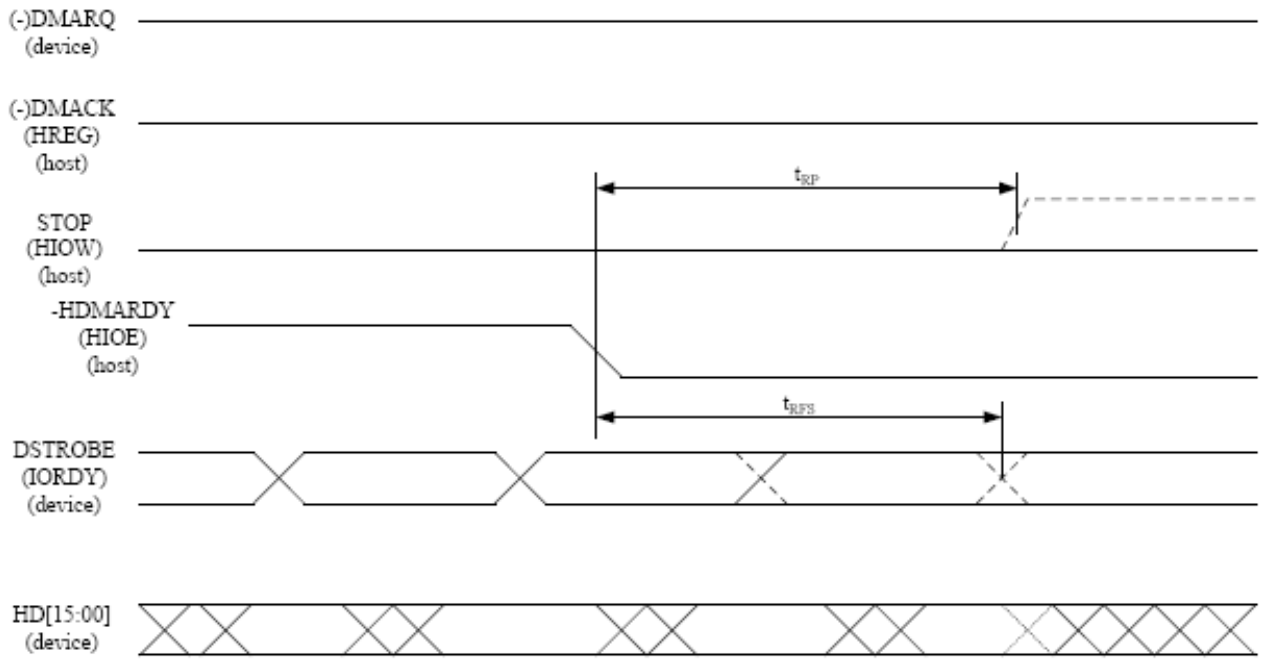

Figure 14: Ultra DMA Data-In Burst Host Pause Timing Diagram

Notes:

1) *All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.*
2) *The host can implement STOP to request termination of the Ultra DMA data burst at a time no sooner than when tRP after HDMARDY# is negated.*
3) *After negating HDMARDY#, the host may receive zero, 1, 2, or 3 additional data words from the device.*
4) *Bus polarities of the DMARQ(#) and DMACK(#) signals are dependent on the active interface mode.*

3.6.17. Ultra DMA Data-In Burst Device Termination Timing

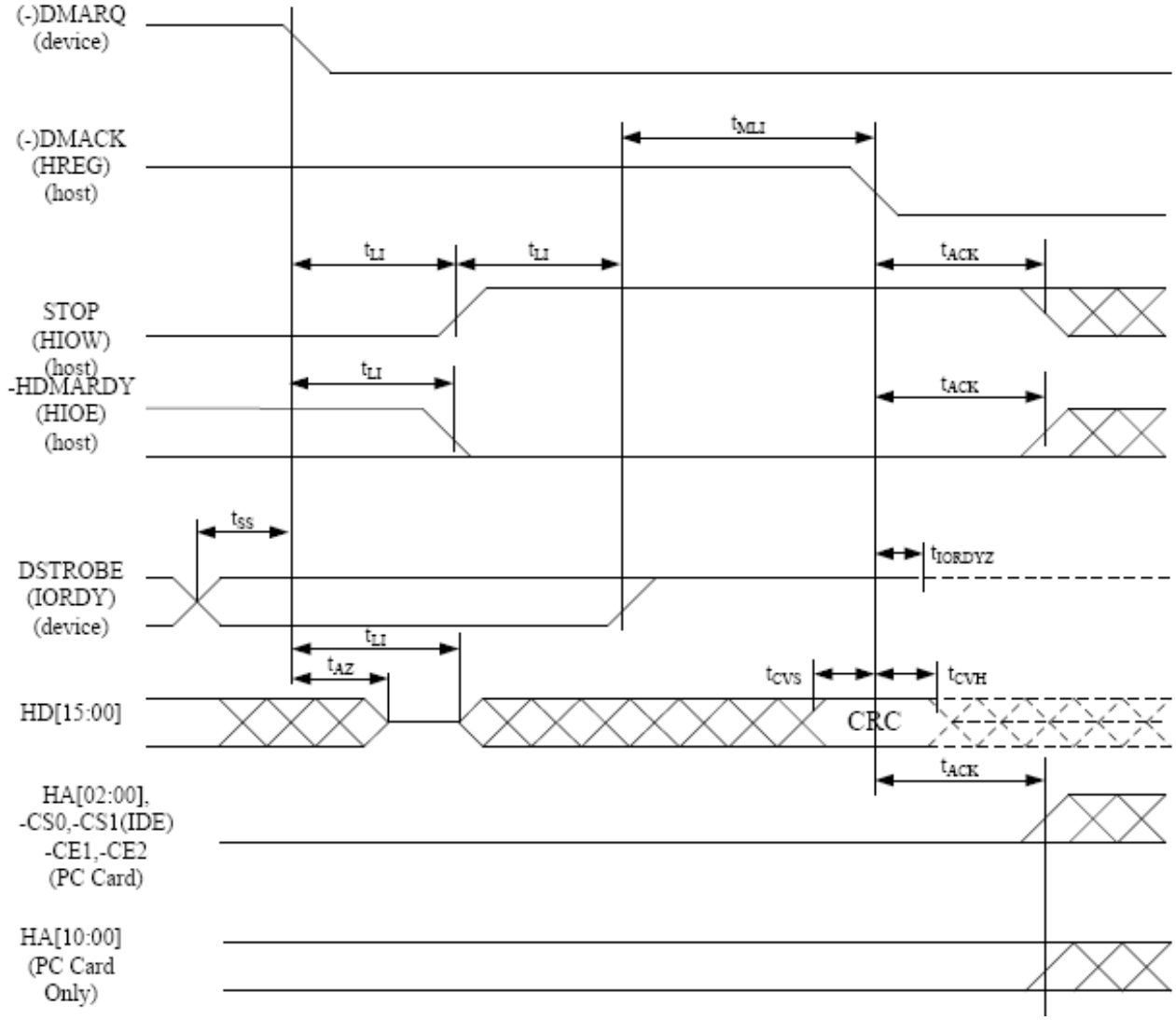

Figure 15: Ultra DMA Data-In Burst Device Termination Timing Diagram

Notes:

1) *All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.*
2) *Definitions for STOP, HDMARDY#, and DSTROBE signal lines are no longer in effect once DMARQ(#) and DMACK(#) are negated. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. HA[10:0], CE1# and CE2# are PC Card mode signals. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.*

3.6.18. Ultra DMA Data-In Burst Host Termination Timing

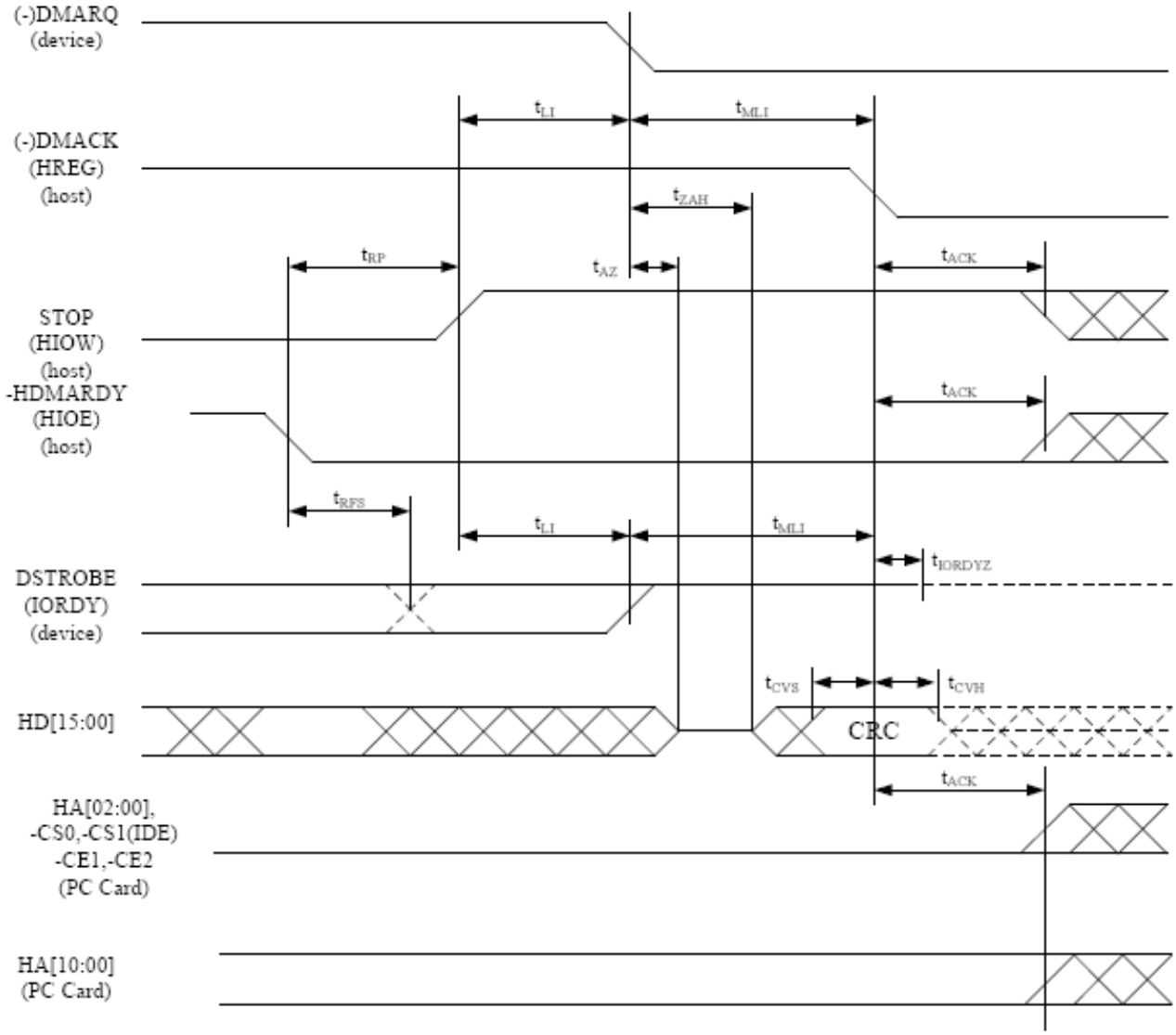

Figure 16: Ultra DMA Data-In Burst Host Termination Timing Diagram

Notes:

1) *All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.*
2) *Definitions for STOP, HDMARDY#, and DSTROBE signal lines are no longer in effect once DMARQ(#) and DMACK(#) are negated. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. The HA[10:0], CE1# and CE2# are PC Card mode signal definitions. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.*

3.6.19. Ultra DMA Data-Out Burst Host Initiation Timing

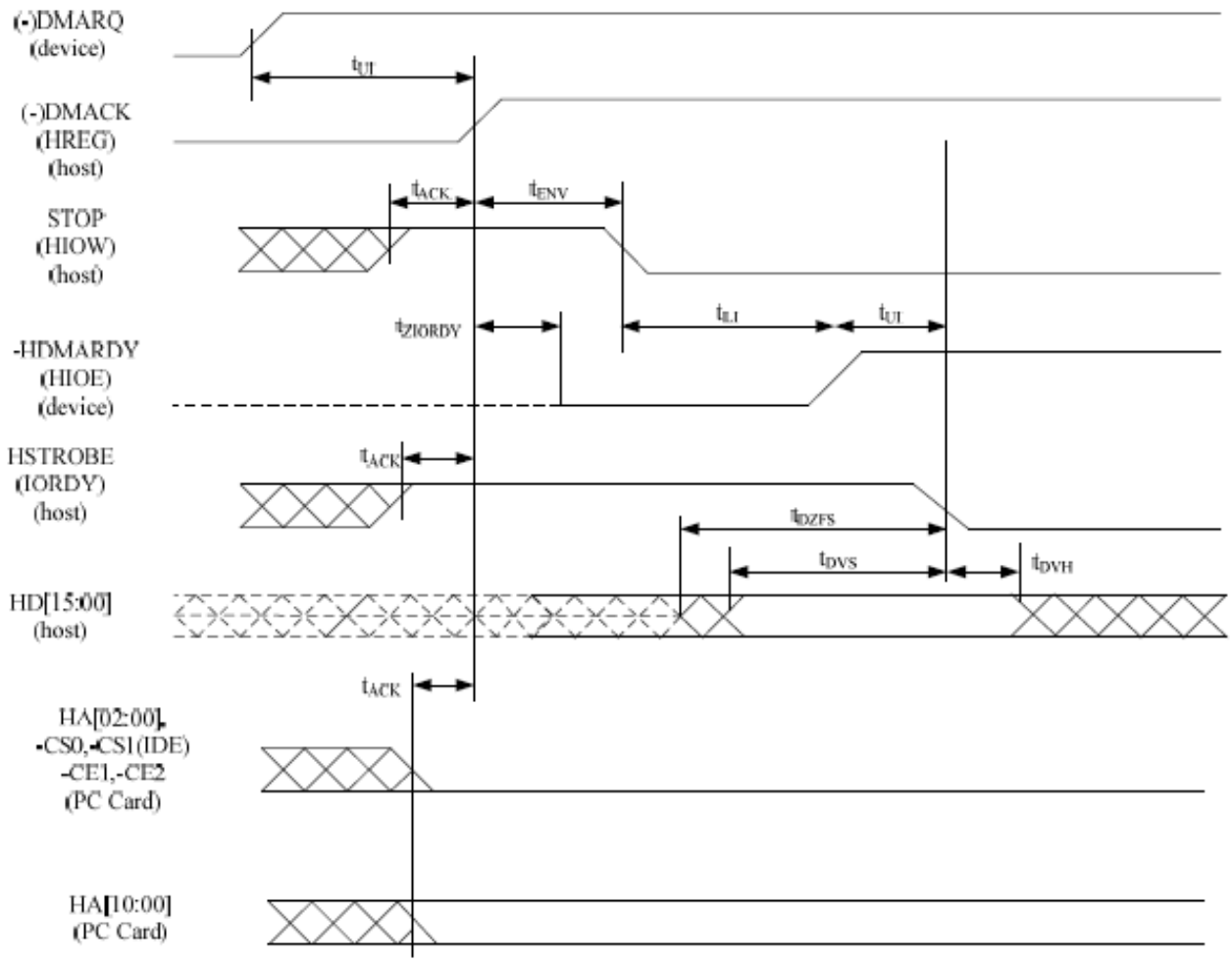

Figure 17: Ultra DMA Data-Out Burst Initiation Timing Diagram

Notes:

1) *All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.*
2) *Definitions for STOP, DDMARDY#, and HSTROBE signal lines are not in effect until the DMARQ(#) and DMACK(#) are asserted. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. The HA[10:0], CE1# and CE2# are PC Card mode signal definitions. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.*

3.6.20. Sustained Ultra DMA Data-Out Burst Host Initiation Timing

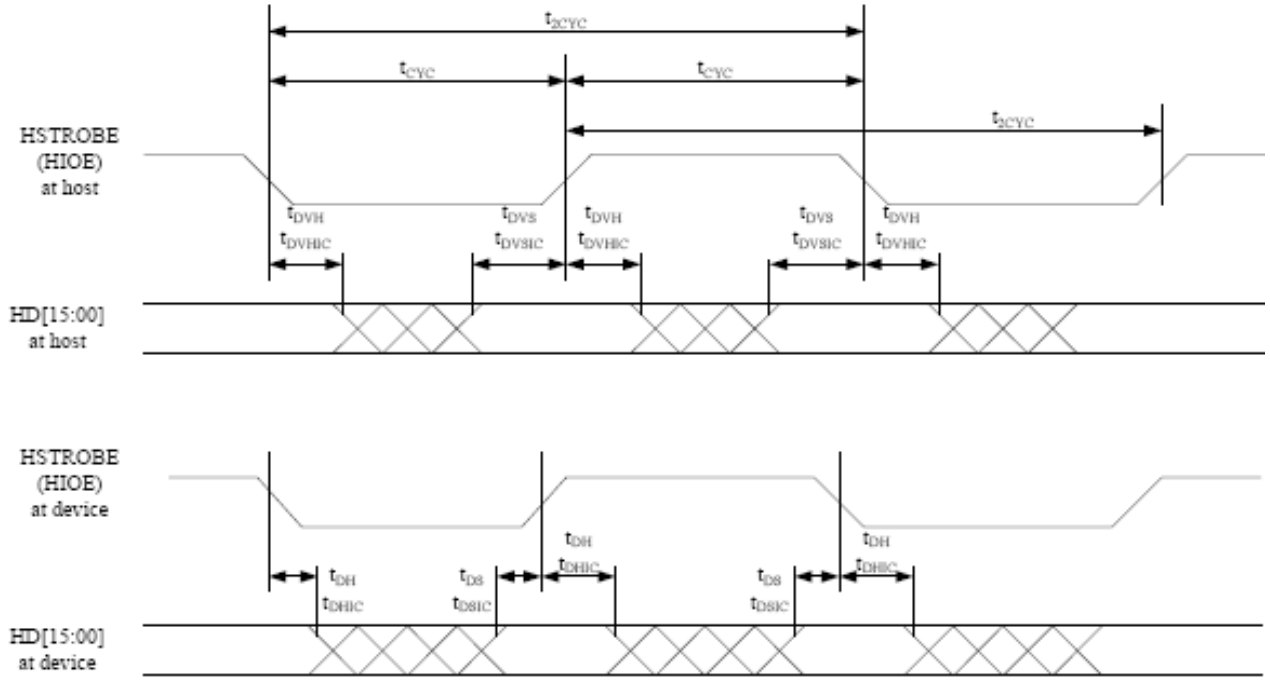

Figure 18: Sustained Ultra DMA Data-Out Burst Timing Diagram

Notes:

Data (HD[15:00]) and HSTROBE signals are shown at both the device and the host to emphasize that cable

Setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until sometime after they are driven by the host.

3.6.21. Ultra DMA Data-Out Burst Device Pause Timing

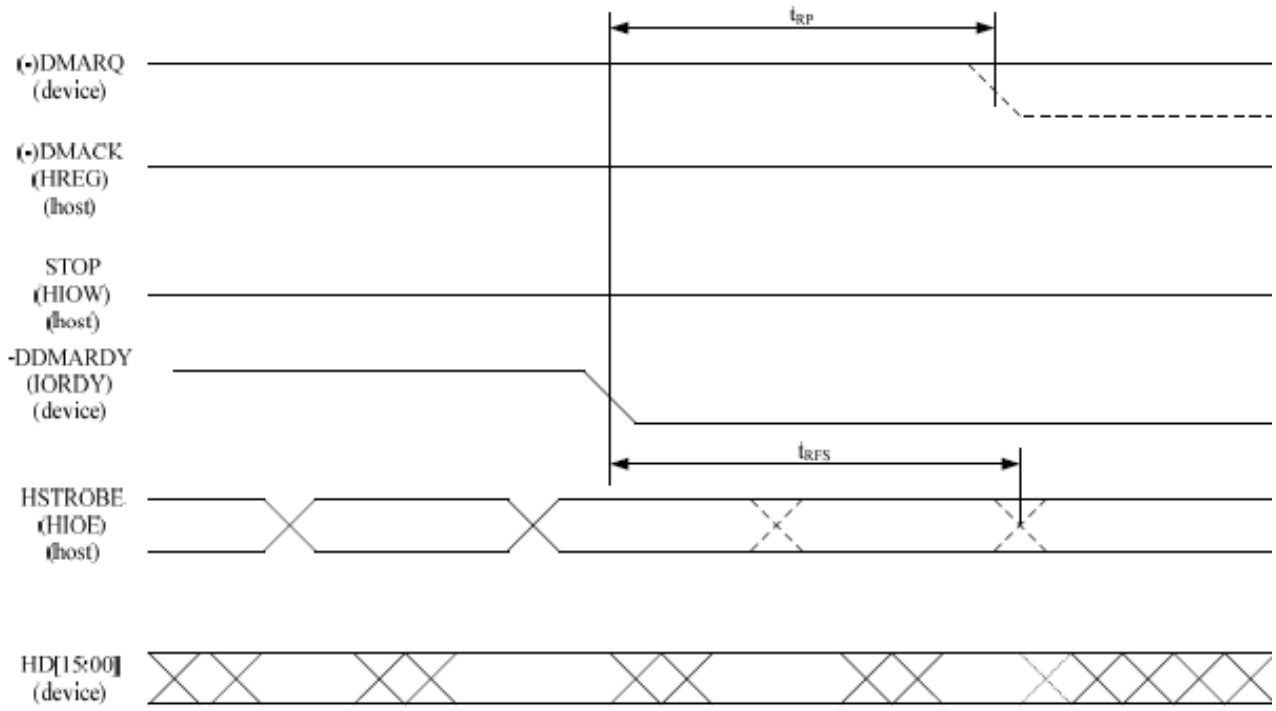

Figure 19: Ultra DMA Data-out Burst Device Pause Timing Diagram

Notes:

1) *All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.*
2) *The device can negate DMARQ(#) when requesting termination of the Ultra DMA data burst no sooner than Trp after DDMARDY# is negated.*
3) *After negating DDMARDY#, the device may receive zero, 1, 2, or 3 additional data words from the host.*
4) *The bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.*

3.6.22. Ultra DMA Data-Out Burst Device Termination Timing

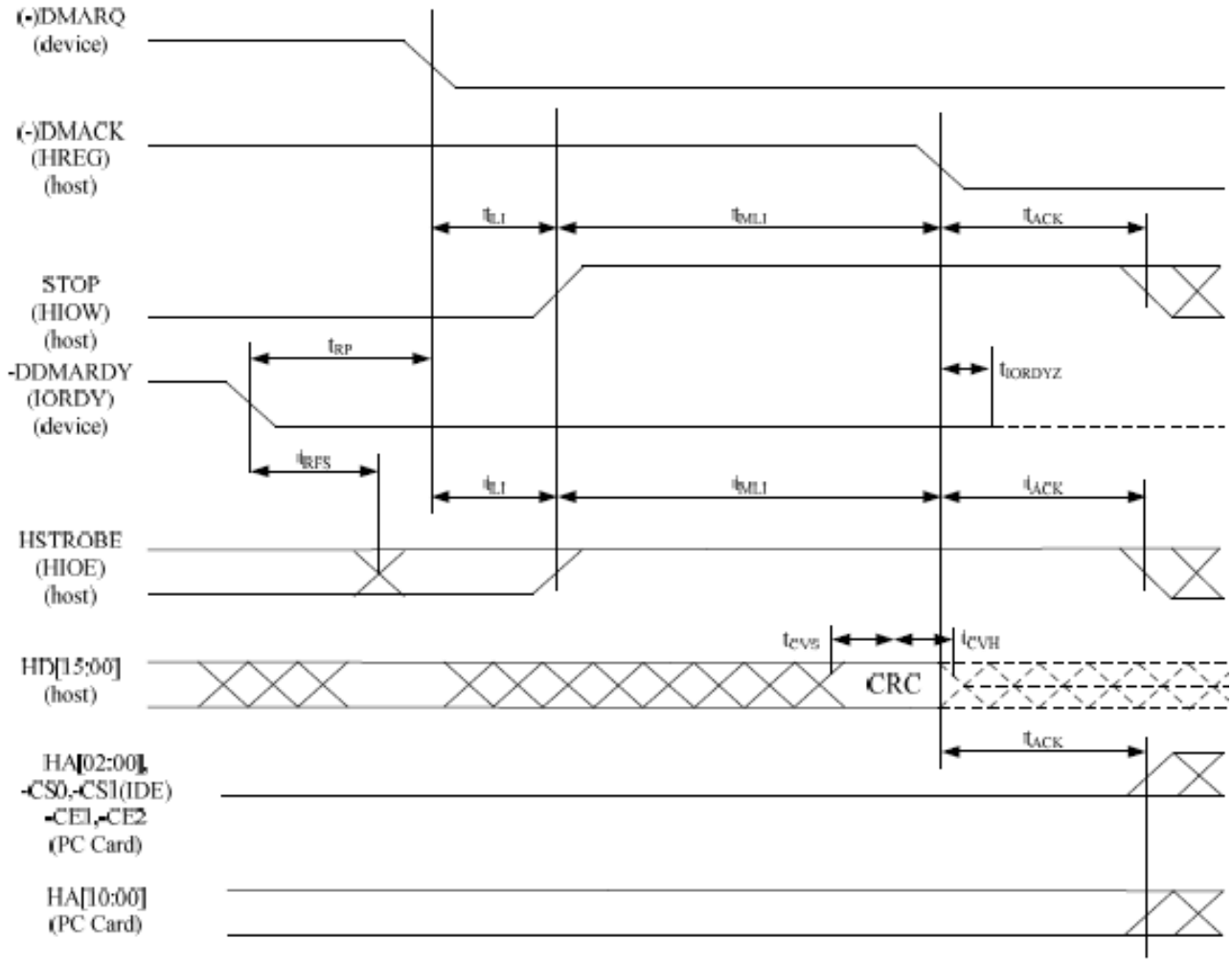

Figure 20: Ultra DMA Data-Out Burst Device Termination Timing Diagram

Notes:

1) *All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.*
2) *Definitions for the STOP, DDMARDY#, and HSTROBE signal lines are no longer in effect [after OR once] DMARQ(#) and DMACK(#) are negated. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. The HA[10:0], CE1# and CE2# are PC Card mode signals. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.*

3.6.23. Ultra DMA Data-Out Burst Host Termination Timing

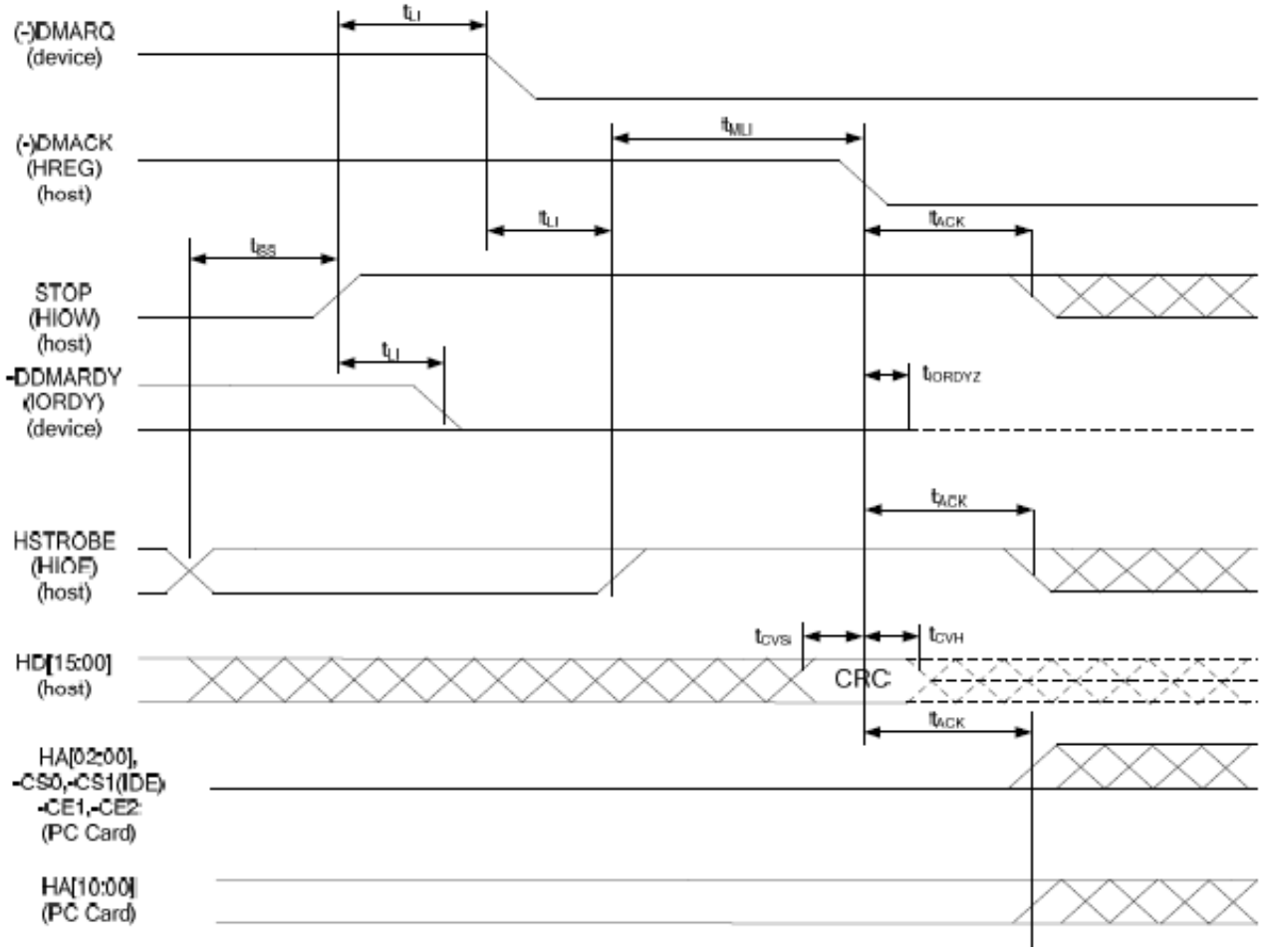

Figure 21: Ultra DMA Data-Out Burst Host Termination Timing Diagram

Notes:

1) *All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.*
2) *Definitions for the STOP, DDMARDY#, and HSTROBE signal lines are no longer in effect once DMARQ(#) and DMACK(#) are negated. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. The HA[10:0], CE1# and CE2# are PC Card mode signal definitions. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.*

4. Transfer Function

4.1. *True IDE Mode I/O Transfer Function*

The APRO industrial CompactFlash (CF) Card HERCULES-N Series can be configured in a True IDE Mode of operation. The APRO industrial CompactFlash (CF) Card HERCULES-N Series is configured in this mode only when –OE input signal is grounded by the host during the power off to power on cycle.

Table 25: True IDE Mode I/O Function

Function Code	-CS1	-CS0	-A0~A2	-DMACK	-IORD	-IOWR	D15~D8	D7~D0
Invalid Mode	L	L	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	L	X	L	Undefined In	Undefined In
	X	L	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	L	X	L	Undefined In	Undefined In
Standby Mode	H	H	X	H	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	H	L	H	High Z	Data In
PIO Data Register Write	H	L	0	H	H	L	Odd-Byte In	Even-Byte In
DMA Data Register Write	H	H	X	L	H	L	Odd-Byte In	Even-Byte In
Ultra DMA Data Register Write	H	H	X	L	See Note 1		Odd-Byte In	Even-Byte In
PIO Data Register Read	H	L	0	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	L	L	H	Odd-Byte Out	Even-Byte Out
Ultra DMA Data Register Read	H	H	X	L	See Note 2		Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	H	L	H	High Z	Status Out
Drive Address	L	H	7h	H	L	H	High Z	Data Out

Note:

1) *In Ultra DMA Data Register Write mode the signals –IORD, -IOWR and IORDY are redefined and used as follows: -IORD as HSTROBE, -IOWR as STOP and IORDY as –DDMARDY. Data transfers with each edge of HSTROBE.*
2) *In Ultra DMA Data Register Read mode the signals –IORD, -IOWR and IORDY are redefined and used as follows: -IORD as –HDMARDY H, -IOWR as STOP and IORDY as DSTROBE. Data transfer with each edge of DSTROBE.*

4.2. *Configuration Register*

4.2.1. Configuration Option Register (200h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the APRO industrial CompactFlash (CF) Card HERCULES-N Series.

Table 26: Configuration Option Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevelREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Table 26: Information for Configuration Option Register

Name	Description
SRSET	Soft Reset: Setting this bit to one (1), waiting the minimum reset time and returning to zero(0) places the APRO industrial CompactFlash (CF) Card HERCULES-N Series in the reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the APRO industrial CompactFlash (CF) Card HERCULES-N Series in the same un-configured, Reset state as following power-up and hardware reset. Contrast with Soft Reset in the Device Control Register.
LevelREQ	This bit is set to one (1) then Level Mode Interrupt is selected, and zero (0) then Pulse Mode is selected. Set to zero (0) by Reset.
Conf5-0	Configuration Index: Set to zero (0) by reset. It is used to select operation mode of the APRO industrial CompactFlash (CF) Card HERCULES-N Series as shown below

Note: Conf5 and Conf4 are reserved for CompactFlash Storage cards and shall be written as zero(0).

4.2.2. Pin Replacement register (204h in Attribute Memory)

Table 27: Pin Replacement Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	Cready	0	1	1	Rready	0
Write	0	0	Cready	0	0	0	Mready	0

Note:

Cready: This bit is set to one (1) when the bit Rready changes state. This bit can also be written by the host.

Rready: This bit is used to determine the internal state of the READY signal. This bit may be used to determine the state of the READY signal as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask (Mready) for writing the corresponding bit Cready.

Mready: This bit acts as a mask for writing corresponding bit Cready.

4.2.3. Socket and Copy Register (206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register. This register is used for identification of the card from the other card.

Table 28: Socket and Copy Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	0	Obsolete (Drive #)	0	0	0	0
Write	0	0	0	Obsolete (Drive #)	X	X	X	X

Note:

Obsolete(Drive #): This bit is obsolete and should be written as 0.

5. Software Specification

5.1. *Addressing of True IDE Mode*

Table 29: True IDE Mode

-CS1	-CS0	A2	A1	A0	-DMACK	-IORD=0	-IOWR=0	Note
1	0	0	0	0	1	PIO RD Data	PIO WR Data	8 or 16 bit
1	1	X	X	X	0	DMA RD Data	DMA WR Data	16 bit
1	0	0	0	1	1	Error Register	Features	8 bit
1	0	0	1	0	1	Sector Count	Sector Count	8 bit
1	0	0	1	1	1	Sector No.	Sector No.	8 bit
1	0	1	0	0	1	Cylinder Low	Cylinder Low	8 bit
1	0	1	0	1	1	Cylinder High	Cylinder High	8 bit
1	0	1	1	0	1	Select Card/Head	Select Card/Head	8 bit
1	1	1	1	1	1	Status	Command	8 bit
0	1	1	1	0	1	Alt Status	Device Control	8 bit

5.2. *CF-ATA Register*

The following section describes the hardware registers used by the host software to issue commands to the APRO industrial CompactFlash (CF) Card HERCULES-N Series.

Note:

In True IDE Mode of operation, the size of the transfer is based solely on the register being addressed. All registers are 8 bit only except for the Data Register, which is normally 16 bits, but can be programmed to use 8 bit transfers for Non-DMA operations through the use of the Set Features command. The data register is also 8 bits during a portion of the Read Long and Write Long commands, which exist solely for historical reasons and should not be used.

5.2.1. Data Register

The Data Register is a 16 bit register, and it is used to transfer data blocks between the card and the host. This register overlaps the Error Register. This register can be accessed in word and byte mode.

Table 30: Data Register

Data Register															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

5.2.2. Error Register

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows.

Table 30: Error Register

BBK	UNC	0	IDNF	0	ABRT	0	AMNF
D7	D6	D5	D4	D3	D2	D1	D0

5.2.3. Feature Register

This register provides information regarding features of the card that the host can utilize. This register is also accessed in PC Card modes on data D15-D8 during a write operation to Offset 0 with –CE2 low and –CE1 high.

Table 31: Feature Register

Feature Register							
D7	D6	D5	D4	D3	D2	D1	D0

5.2.4. Sector Count Register

This registers the number of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

Table 32: Sector Count Register

Sector Count Register							
D7	D6	D5	D4	D3	D2	D1	D0

5.2.5. Sector Number Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for APRO industrial CompactFlash (CF) Card HERCULES-N Series data access for the subsequent command.

Table 33: Sector Number Register

Sector Number Register							
D7	D6	D5	D4	D3	D2	D1	D0

5.2.6. Cylinder Low Register

This Register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

Table 34: Cylinder Low Register

Cylinder Low Register							
D7	D6	D5	D4	D3	D2	D1	D0

5.2.7. Cylinder High Register

This Register contains the high order 8 bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

Table 35: Cylinder High Register

Cylinder High Register							
D7	D6	D5	D4	D3	D2	D1	D0

5.2.8. Device/Head Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing.

Table 36: Device/Head Register

1	LBA	1	DRV	HS3	HS2	HS1	HS0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: this bit is set 1.

Bit6: LBA is a flag to select either Cylinder/Head/Sector or Logical Block Address mode. When LBA=0, Cylinder/ Head/ Sector mode is selected. When LBA=1, Logical Block Address is selected.

Bit5: this bit is set 1.

Bit4: DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected.

Bit3: When operation in the Cylinder/Head/Sector mode, this is bit 3 of the head number. It is bit 27 in the Logical Block Address mode.

Bit2: When operation in the Cylinder/Head/Sector mode, this is bit 2 of the head number. It is bit 26 in the Logical Block Address mode.

Bit1: When operation in the Cylinder/Head/Sector mode, this is bit 1 of the head number. It is bit 25 in the Logical Block Address mode.

Bit0: When operation in the Cylinder/Head/Sector mode, this is bit 0 of the head number. It is bit 24 in the Logical Block Address mode.

5.2.9. Status Register

These registers return the APRO industrial CompactFlash (CF) Card HERCULES-N Series status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not.

Table 37: Status Register

BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: the busy bit is set when the APRO industrial CompactFlash (CF) Card HERCULES-N Series has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit set to a 1.

Bit6: RDY indicates whether the device is capable of performing APRO industrial CompactFlash (CF) Card HERCULES-N Series operations. This bit is cleared at power up and remains cleared until the card is ready to accept a command.

Bit5: This bit, if set, indicates a write fault has occurred.

Bit4: This bit is set when the APRO industrial CompactFlash (CF) Card HERCULES-N Series is ready.

Bit3: The Data Request is set when the APRO industrial CompactFlash (CF) Card HERCULES-N Series requires that information be transferred either to or from the host through the Data register.

During the data transfer of DMA commands, the card shall not asserted DMARD unless either the BUST bit, the DRQ, or both are set to one.

Bit2: This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit1: This bit is always to 0.

Bit0: This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information description the error.

5.2.10. Device Control Register

This register is used to control the APRO industrial CompactFlash (CF) Card HERCULES-N Series interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY.

Table 38: Device Control Register

X	X	X	X	X	SW Rst	-Ien	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7-3: These bits are ignored.

Bit2: This bit is set to 1 in order to force the APRO industrial CompactFlash (CF) Card HERCULES-N Series to perform a Soft Reset operation. The Card remains in Reset until this bit is reset to ‘0’.

Bit1: the Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupt from the APRO industrial CompactFlash (CF) Card HERCULES-N Series are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.

Bit0: This bit is ignored.

5.2.11. Drive Address Register

This register is provide for compatibility with the AT disk drive interface.

Table 39: Drive Address Register

X	-WTG	-HS3	-HS2	-HS1	-HS0	-Nds1	-Nds0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: this bit is unknown.

Bit6: this bit is – when a write operation is in progress; otherwise, it is 1.

Bit5: this bit is the negation of bit 3 in the Drive/Head register.

Bit4: this bit is the negation of bit 2 in the Drive/Head register.

Bit3: this bit is the negation of bit 1 in the Drive/Head register.

Bit2: this bit is the negation of bit 0 in the Drive/Head register.

Bit1: this bit is 0 when drive 1 is active and selected.

Bit0: this bit is 0 when the drive 0 is active and selected.

5.3. *Hardware Reset*

Table 40: Timing Diagram, Hardware Reset

	Item	Min.	Max.	Normal	Unit
t_{SU}(RESET)	Reset Setup Time	20	-	-	ms
t_{REC}(VCC)	-CE Recover Time	1	-	-	us
t_{PR}	VCC rising up time	0.1	100	-	ms
t_{PF}	VCC falling down time	3	300	-	ms
t_{W}(RESET)	Reset pulse width	10	-	-	ms
t_{H}(Hi-ZRESET)		0	-	-	
t_{S}(Hi-ZRESET)		0	-	-	

5.4. *Power on Reset*

When the VCC power reaches to 2.7V, the disk drive will be reset.

Table 41: Timing Diagram, Power On Reset

	Item	Min.	Max.	Normal	Unit	Note
t_{SU}(RESET)	-CE Setup Time	20	-	-	ms	
t_{PR}	-VCC Rising Up Time	0.1	100	-	ms	

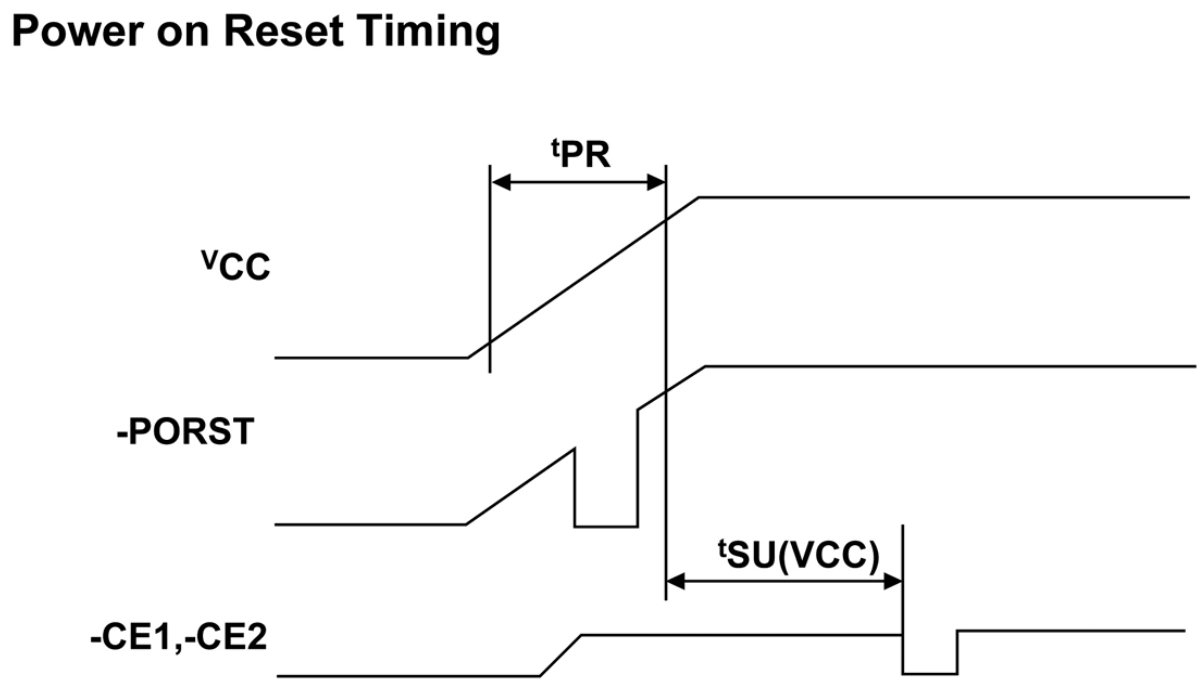

Figure 22: Timing Diagram, Power On Reset

5.5. *ATA Command Set*

The following table summarizes the commands supported by the controller.

Table 43: ATA Command Set

Command	Code	FR	SC	SN	CY	DH	LBA
Check Power Mode	E5H	-	-	-	-	D	-
Execute Device Diagnostic	90H	-	-	-	-	D	-
Flush Cache	E7H	-	-	-	-	Y	-
Identify Device	ECH	-	-	-	-	D	-
Idle	E3H	-	Y	-	-	D	-
Idle immediate	E1H	-	-	-	-	D	-
Read Buffer	E4H	-	-	-	-	D	-
Read DMA	C8H	-	Y	Y	Y	Y	Y
Read Sector(s)	20H	-	Y	Y	Y	Y	Y
Read Verify Sector(s)	40H	-	Y	Y	Y	Y	Y
Set Features	EFH	Y	-	-	-	D	-
Set Multiple Mode	C6H	-	Y	-	-	D	-
Set Sleep Mode	E6H	-	-	-	-	D	-

SMART	B0h	Y	-	-	Y	Y	-
Standby	E2H	-	-	-	-	D	-
Standby Immediate	E0H	-	-	-	-	D	-
Write Buffer	E8H	-	-	-	-	D	-
Write DMA	CAH	-	Y	Y	Y	Y	Y
Write Multiple	C5h	-	Y	Y	Y	Y	Y
Write Sector(s)	30H	-	Y	Y	Y	Y	Y

Notes:

1) *These commands are optional, depending on the key Management scheme in use.*
2) *Use of this command is not recommended by CFA.*
3) *Use of this command is not recommended.*
4) *SM223 don't have cache.*
5) *Will support by firmware update, it will be available by September, 2007*
6) *Definitions*

FR = Features Register

SC =Sector Count register (00H to FFH, 00H means 256 sectors) S

N = Sector Number register

CY = Cylinder Low/High register

DH = Head No. (0 to 15) of Drive/Head register

LBA = Logic Block Address Mode Support

– = Not used for the command

Y = Used for the command

5.6. *ATA Command Description*

(1) CFA Erase Sector(s) – C0h

This command pre-erases and conditions from 1 to 256 sectors in the Sector Count register. This command must be issued in advance of CFA Write without Erase or CFA Write Multiple without Erase command to increase the execution speed of the write operation.

(2) CFA Request Extended Error Code – 03h

This command requests extended error information for the previous command. The extended error code is returned to the host in the Error Register.

(3) CFA Translate Sector – 87h

This command allows the host a method of determining the exact times a user sector has been erased and programmed. This controller will respond with a 512-byte buffer of information containing the desired cylinder, head and sector, including its Logical Address.

(4) CFA Write Multiple w/o Erase – CDh

This command is similar to Write Multiple command with the exception that an implied erase before write operation is not performed.

(5) Write Sector(s) w/o Erase – 38h

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed.

(6) Check Power Mode – E5h

This command checks the power mode. If the CompactFlash Storage is in, going to, or recovering from the sleep mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt. If the ompactFlash Storage Card is in idle mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

(7) Flush Cache- E7h

Command Code: E7h

Protocol: Non-data

Inputs:

Table 44: Flush cache command for inputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E7h							

Device register–

DEV shall specify the selected device.

Normal Output

Table 45: Flush cache command for normal output information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							

Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

Table 46: Flush cache command for error output information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY will be set to one.

Description

This command is used by the host to request the device to flush the write cache. If there is data in write cache, that data shall be written to the SSD. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

(8) Execute Device Diagnostic – 90h

This command performs the internal diagnostic tests implemented by the CompactFlash Storage Card. When the diagnostic command is issued in the True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices. The Diagnostic codes are shown in Table 34. Diagnostic Codes are returned in the Error Register at the end of the command.

Table 47: Diagnostic

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controller Microprocessor Error
8Xh	Slave Error in True IDE Mode

(9) Identify Device – ECh

The Identify Device command enables the host to receive parameter information from the CompactFlash Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 35. All reserved bits or words are zero. Hosts should not depend in Obsolete words in Identify Device containing 0. Table 35 specifies each filed in the data returned by the Identify Device Command. In Table 35, X indicates a numeric nibble vale specific to the card and aaaa indicates an ASCII string specific to the particular drive.

Table 48: IDENTIFY DEVICE information

Word	Description	Value
0	General configuration bit-significant information: 15 0 = ATA device 14-8 Retired 7 1 = removable media device 6 Obsolete 5-3 Retired 2 Response incomplete 1 Retired 0 Reserved	044Ah
1	Obsolete	XXXXh
2	Specific configuration	0000h
3	Obsolete	00XXh
4-5	Retired	XXXXh

6	Obsolete	XXXXh
7-8	Reserved for assignment by the CompactFlash™ Association	XXXXh
9	Retired	0000h
10-19	Serial number (20 ASCII characters)	20 ASCII characters
20-21	Retired	0002h
22	Obsolete	0004h
23-26	Firmware revision (8 ASCII characters)	8 ASCII characters
27-46	Model number (40 ASCII characters)	40 ASCII characters
47	80h 15-8 00h = Reserved 7-0 01h-FFh = Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands	8001h
48	Reserved	0000h
49	Capabilities 15-14 Reserved for the IDENTIFY PACKET DEVICE command. 13 1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device 12 Reserved for the IDENTIFY PACKET DEVICE command. 11 1 = IORDY supported 0 = IORDY may be supported 10 1 = IORDY may be disabled 9 1 = LBA supported 8 1 = DMA supported. 7-0 Retired	0F00h
50	Capabilities 15 Shell be cleared to zero 14: Shall be set to one 13-2 Reserved 1 Obsolete 0 Shall be set to one to indicate a device specific Standby timer value minimum.	0000h
51	Obsolete	0200h
52	Obsolete	0000h
53	15-3 Reserved	0007h

	2 1 = the fields reported in word 88 are valid Reserved 0 = the fields reported in word 88 are not valid 1 1 = the fields reported in words (70:64) are valid 0 = the fields reported in words (70:64) are not valid 0 Obsolete	
54	Number of current logical cylinders	XXXXh
55	Number of current logical heads	XXXXh
56	Number of current logical sectors per logical track	XXXXh
57-58	Current capacity in sectors	XXXXh
59	15-9 Reserved 8 1 = Multiple sector setting is valid 7-0 xxh = Current setting for number of sectors that shall be transferred per interrupt on R/W Multiple command	01XXh
60-61	Total number of user addressable sectors	XXXXXXXXh
62	Obsolete	0000h
63	15-11 Reserved 10 1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected 9 1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected 8 1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected 7-3 Reserved 2 1 = Multiword DMA mode 2 and below are supported 1 1 = Multiword DMA mode 1 and below are supported 0 1 = Multiword DMA mode 0 is supported	XX07h
64	15-8 Reserved 7-0 PIO modes supported	0003h
65	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds	0078h
66	Manufacturer's recommended Multiword DMA transfer cycle time 15-0 Cycle time in nanoseconds	0078h
67	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds	0078h
68	Minimum PIO transfer cycle time with IORDY flow control	0078h

	15-0 Cycle time in nanoseconds	
69-70	Reserved (for future command overlap and queuing)	0000h
71-74	Reserved for the IDENTIFY PACKET DEVICE command.	0000h
75	Queue depth 15-5 Reserved 4-0 Maximum queue depth - 1	0000h
76-79	Reserved for Serial ATA	0000h 0000h 0000h 0000h
80	Major version number 0000h or FFFFh = device does not report version 15 Reserved 14 Reserved for ATA/ATAPI-14 13 Reserved for ATA/ATAPI-13 12 Reserved for ATA/ATAPI-12 11 Reserved for ATA/ATAPI-11 10 Reserved for ATA/ATAPI-10 9 Reserved for ATA/ATAPI-9 8 Reserved for ATA/ATAPI-8 7 1 = supports ATA/ATAPI-7 6 1 = supports ATA/ATAPI-6 5 1 = supports ATA/ATAPI-5 4 1 = supports ATA/ATAPI-4 3 Obsolete 2 Obsolete 1 Obsolete 0 Reserved	0080h
81	Minor version number 0000h or FFFFh = device does not report version 0001h-FFFEh = See 6.17.41	0000h
82	Command set supported. 15 Obsolete 14 1 = NOP command supported 13 1 = READ BUFFER command supported 12 1 = WRITE BUFFER command supported	742Bh

	11	Obsolete	
	10	1 = Host Protected Area feature set supported	
	9	1 = DEVICE RESET command supported	
	8	1 = SERVICE interrupt supported	
	7	1 = release interrupt supported	
	6	1 = look-ahead supported	
	5	1 = write cache supported	
	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.	
	3	1 = mandatory Power Management feature set supported	
	2	1 = Removable Media feature set supported	
	1	1 = Security Mode feature set supported	
	0	1 = SMART feature set supported	
83	Command sets supported.		5100h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = FLUSH CACHE EXT command supported	
	12	1 = mandatory FLUSH CACHE command supported	
	11	1 = Device Configuration Overlay feature set supported	
	10	1 = 48-bit Address feature set supported	
	9	1 = Automatic Acoustic Management feature set supported	
	8	1 = SET MAX security extension supported	
	7	See Address Offset Reserved Area Boot, INCITS TR27:2001	
	6	1 = SET FEATURES subcommand required to spinup after power-up	
	5	1 = Power-Up In Standby feature set supported	
	4	1 = Removable Media Status Notification feature set supported	
	3	1 = Advanced Power Management feature set supported	
	2	1 = CFA feature set supported	
	1	1 = READ/WRITE DMA QUEUED supported	
	0	1 = DOWNLOAD MICROCODE command supported	
84	Command set/feature supported extension		4003h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported	
	12	Reserved for technical report	
	11	Reserved for technical report	

	10	1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT	
	9	1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT	
	8	1 = 64-bit World wide name supported	
	7	1 = WRITE DMA QUEUED FUA EXT command supported	
	6	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported	
	5	1 = General Purpose Logging feature set supported	
	4	1 = Streaming feature set supported	
	3	1 = Media Card Pass Through Command feature set supported	
	2	1 = Media serial number supported	
	1	1 = SMART self-test supported	
	0	1 = SMART error logging supported	
85	Command and feature sets supported or enabled		
	15	Obsolete	0
	14	1 = NOP command enabled	0
	13	1 = READ BUFFER command enabled	0
	12	1 = WRITE BUFFER command enabled	0
	11	Obsolete	0
	10	1 = Host Protected Area feature set enabled	1
	9	1 = DEVICE RESET command enabled	0
	8	1 = SERVICE interrupt enabled	0
	7	1 = release interrupt enabled	0
	6	1 = look-ahead enabled	0
	5	1 = Write Cache enabled	1
	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.	0
	3	1 = Power Management feature set enabled	0
	2	1 = Removable Media feature set enabled	0
	1	1 = Security Mode feature set enabled	X
	0	1 = SMART feature set enabled	X
86	Command set/feature enabled		
	15-14	0 = Reserved	1000h
	13	1 = FLUSH CACHE EXT command supported	
	12	1 = FLUSH CACHE command supported	

	11	1 = Device Configuration Overlay supported	
	10	1 = 48-bit Address features set supported	
	9	1 = Automatic Acoustic Management feature set enabled	
	8	1 = SET MAX security extension enabled by SET MAX SET PASSWORD	
	7	See Address Offset Reserved Area Boot, INCITS TR27:2001	
	6	1 = SET FEATURES subcommand required to spin-up after power-up	
	5	1 = Power-Up In Standby feature set enabled	
	4	1 = Removable Media Status Notification feature set enabled	
	3	1 = Advanced Power Management feature set enabled	
	2	1 = CFA feature set enabled	
	1	1 = READ/WRITE DMA QUEUED command supported	
	0	1 = DOWNLOAD MICROCODE command supported	
87	Command and feature sets supported or enabled		0003h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported	
	12	Reserved for technical report-	
	11	Reserved for technical report-	
	10	1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT	
	9	1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT	
	8	1 = 64 bit World wide name supported	
	7	1 = WRITE DMA QUEUED FUA EXT command supported	
	6	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported	
	5	1 = General Purpose Logging feature set supported	
	4	1 = Valid CONFIGURE STREAM command has been executed	
	3	1 = Media Card Pass Through Command feature set enabled	
	2	1 = Media serial number is valid	
	1	1 = SMART self-test supported	
	0	1 = SMART error logging supported	
88	15	Reserved	XX7Fh
	14	1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected	
	13	1 = Ultra DMA mode 5 is selected	

	12	0 = Ultra DMA mode 5 is not selected 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected	
	11	1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected	
	10	1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected	
	9	1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected	
	8	1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected	
	7	Reserved	
	6	1 = Ultra DMA mode 6 and below are supported	
	5	1 = Ultra DMA mode 5 and below are supported	
	4	1 = Ultra DMA mode 4 and below are supported	
	3	1 = Ultra DMA mode 3 and below are supported	
	2	1 = Ultra DMA mode 2 and below are supported	
	1	1 = Ultra DMA mode 1 and below are supported	
	0	1 = Ultra DMA mode 0 is supported	
89	Time required for security erase unit completion		0001h
90	Time required for Enhanced security erase completion		0000h
91	Current advanced power management value		0000h
92	Master Password Revision Code		FFFEh
93	Hardware reset result. The contents of bits (12:0) of this word shall change only during the execution of a hardware reset. 15 Shall be cleared to zero. 14 Shall be set to one. 13 1 = device detected CBLID- above ViH 0 = device detected CBLID- below ViL		XXXXh

		Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows: 12 Reserved. 11 0 = Device 1 did not assert PDIAG-. 1 = Device 1 asserted PDIAG-. 12-8 10-9 These bits indicate how Device 1 determined the device number: 00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown. 8 Shall be set to one.	
		Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows: 7 Reserved. 6 0 = Device 0 does not respond when Device 1 is selected. 1 = Device 0 responds when Device 1 is selected. 5 0 = Device 0 did not detect the assertion of DASP-. 1 = Device 0 detected the assertion of DASP-. 4 0 = Device 0 did not detect the assertion of PDIAG-. 7-0 1 = Device 0 detected the assertion of PDIAG-. 3 0 = Device 0 failed diagnostics. 1 = Device 0 passed diagnostics. 2-1 These bits indicate how Device 0 determined the device number: 00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown. 0 Shall be set to one.	
94	15-8	Vendor's recommended acoustic management value.	0000h
	7-0	Current automatic acoustic management value.	
95	Stream Minimum Request Size		0000h
96	Streaming Transfer Time - DMA		0000h
97	Streaming Access Latency - DMA and PIO		0000h
98-99	Streaming Performance Granularity		0000h
100-103	Maximum user LBA for 48-bit Address feature set.		0000h
104	Streaming Transfer Time - PIO		0000h
105	Reserved		0000h

106	Physical sector size / Logical Sector Size 15 Shall be cleared to zero 14 Shall be set to one 13 1 = Device has multiple logical sectors per physical sector. 12 1= Device Logical Sector Longer than 256 Words 11-4 Reserved 3-0 2^X logical sectors per physical sector	0000h
107	Inter-seek delay for ISO-7779 acoustic testing in microseconds	0000h
108	15-12 NAA (3:0) 11-0 IEEE OUI (23:12)	0000h
109	15-4 IEEE OUI (11:0) 3-0 Unique ID (35:32)	0000h
110	15-0 Unique ID (31:16)	0000h
111	15-0 Unique ID (15:0)	0000h
112-115	Reserved for world wide name extension to 128 bits	0000h
116	Reserved for technical report-	0000h
117-118	Words per Logical Sector	0000h
119-120	Reserved	0000h
121-126	Reserved	0000h
127	Removable Media Status Notification feature set support 15-2 Reserved 1-0 00 = Removable Media Status Notification feature set not supported 01 = Removable Media Status Notification feature supported 10 = Reserved 11 = Reserved	0000h
128	Security Status 15-9 Reserved 8 Security level 0 = high, 1 = Maximum 7-6 Reserved 5 1= Enhanced security erase supported 4 1= Security count expired 3 1 = Security frozen 2 1 = Security locked 1 1 = Security enabled 0 1 = Security supported	0 X 0 0 0 X X X 1
129-159	Vendor specific	0000h

160	CFA power mode 1 15 Word 160 supported 14 Reserved 13 CFA power mode 1 is required for one or more commands implemented by the device 12 CFA power mode 1 disabled 11-0 Maximum current in ma	0000h
161-175	Reserved for assignment by the CompactFlash™ Association	0000h
176-205	Current media serial number	0000h
206-254	Reserved	0000h
255	Integrity word 15-8 Checksum 7-0 Signature	XXXXh

(10) Idle -97H or E3H

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

Table 49: Idle information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command(7)	97h or E3h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Timer Count (5 msec increments)							
Feature(1)	X							

(11) Idle immediate - 95H or E1H

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt.

Table 50: Idle immediate information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command(7)	95h or E1h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							

Cylinder Low(4)	X
Sector Number(3)	X
Sector Count(2)	X
Feature(1)	X

(12) Read Buffer - E4h

The Read Buffer command enables the host to read the current contents of the CompactFlash Storage Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

Table 51: Read buffer information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command(7)	E4h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

(13) Read DMA – C8h

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 request 256 sectors. The transfer begins at he sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, cleat BSY. The Card asserts DMAREQ while data is available to be transferred. The Card asserts DMAREQ while data is available to be transferred. The host then reads the (512 & sector –count) bytes of data from the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts –DMACK while it is ready to transfer data by DMA and asserts –IORD once for each 16 bit word to be transferred to the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder, head, and sector number of the sector where the occurred. The amount of data transferred is indeterminate. When a Read DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

Table 52: Read DMA information

Register	7	6	5	4	3	2	1	0
Command(7)	C8h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16							
Cylinder Low(4)	Cylinder Low (LBA 15-8							
Sector Number(3)	Sector Numbe(LBA 7-0							
Sector Count(2)	Sector Count							
Feature(1)	X							

(14) Read Sector(s) - 20h

This command reads from 1 to 256 sectors as specified in the Sector Count Register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has buffer, sets DRQ, cleats BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder head, and sector number of the sector 2where the error occurred. The flawed data is pending in the sector buffer.

Table 53: Read sector information

Register	7	6	5	4	3	2	1	0
Command(7)	20h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

(15) Read Verify Sector(s) – 40h

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash Storage Card sets BSY. When the requested sectors have been verified, the CompactFlash Storage Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified. If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count

Register contains the number of sectors not yet verified.

Table 54: Read verify sector information

Register	7	6	5	4	3	2	1	0
Command(7)	40h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

(16) Set Features - Efh

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the CompactFlash Storage Card shall return command aborted.

Table 55: Set feature information

Register	7	6	5	4	3	2	1	0
Command(7)	Efh							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Config							
Feature(1)	Feature							

Table 56: Feature Supported

Command Name	Code	Sub Command
Set Transfer Mode	Efh	03h
Disable Read Look-ahead feature	Efh	55h
Enable write cache	Efh	02h
Disable reverting to power-on defaults	Efh	66h
Disable write cache	Efh	82h
Enable reverting to power-on defaults	Efh	CCh

(17) Set Multiple Mode – C6h

This command enables the CompactFlash Storage Card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the CompactFlash Storage Card sets BSY to 1 and checks the Sector Count Register. If the Sector Count Register contains a valid value and the block count is supported, the value is

loaded and execution is enabled for all subsequent Read Multiple and Write Multiple commands. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write multiple disabled.

Table 57: Set multiple mode information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command(7)	C6h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Sector Count							
Feature(1)	X							

(18) Sleep – E6h

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds.

Table 58: Set sleep mode information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command(7)	E6h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

(19) Standby – E2h

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, cleat BSY and return interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

(20) Standby Immediate – E0h

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

(21) Write Buffer – E8h

The Write Buffer command enables the host to overwrite contents of the CompactFlash Storage Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfer 512 bytes.

(22) Write DMA – CAh

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The host then writes the (512*sector count) bytes of data to the Card using DMA. While DMAREQ is asserted by the Card, the host asserts –DMACK while it is ready to transfer data by DMA and asserts –IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecovertable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The amount of data transferred is indeterminate. When a write DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

Table 59: Write DMA information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command(7)	Cah							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low(LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

(23) Write Multiple – C5h

Command Code: C5h

Protocol: PIO data-out

Inputs

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 60: Write multiple command for inputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C5h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

Normal Output

Table 61: Write multiple command for normal output information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block register contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 62: Write multiple command for normal output information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range user-accessible address is requested if command aborted is not returned.

ABRT shall be set to one if an error, include an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if an address outside of the range of user-accessible address is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device -

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one. If bit 8 of IDENTIFY DEVICE word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

Description

This command writes the number of sectors specified in the Sector Count register.

The number of sectors per block is defined by the content of word 59 of the IDENTIFY DEVICE response.

When the WRITE MULTIPLE command is issued, the SECTOR Count register contains the number of sectors (not the number of blocks) requested. The device shall interrupt for each DRQ block transferred.

IF the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

N = Remainder (sector count / block count).

If the WRITE MULTIPLE command is received when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with command aborted.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The command ends with the sector in error, even if the error was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupt pending is set when the DRQ bit is set to one at the beginning of each block or partial block.

(24) Write Sector(s) – 30h

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the CompactFlash Storage Card sets BST, then sets DRQ and clears BSDY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

Table 63: Write sector information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command(7)	30h							
C/D/H(6)	1	LBA	1	Drive	Head(LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

(25) Security Set Password- F1h

Command Code: F1h

Feature Set: Security Mode feature set

Protocol: PIO data-out

Inputs

Table 64: Security set password command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F1h							

Device –

DEV shall specify the selected device.

Normal Outputs

Table 65: Security set password command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

Error Outputs

Table 66: Security set password command for error outputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command transfer 512 byte of data from the host. Table 10 defines the content of this information. The data transferred controls the function of this command. Table 11 defines the interaction of the identifier and security level bits.

The revision code field shall be returned in the IDENTIFY DEVICE word 92. The valid revision codes are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision Code is not supported.

Table 67: Security set password command's data content

Word	**Content**
0	Control Word Bit 0 Identifier 0=set User password 1=set Master password Bits (7:1) Reserved Bit(8) Security level 0=High 1=Maximum Bits(15:9) Reserved
1-16	Password(32 bytes)

17	Master Password Revision Code()
18-255	Reserved

Table 68: Security Set password command's identifier and security level bit interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall than be unlocked by either the User password it the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by only the User password. The Master password previously set is still stored in the device but shall not be unlock
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed. Master password revision code set to the value in Master Password Revision Code field.

(26) Security Unlock- F2h

Command Code: F2h

Feature Set: Security Mode feature set

Protocol: PIO data-out

Inputs

Table 69: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F2h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 70: Security unlock command for inputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

Error Outputs

The device shall return aborted if the device is in Frozen mode.

Table 71: Security unlock command for inputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command transfers 512 bytes of data from the host. Table13 defines the content of this information. If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the Identifier bit is set to user then the device shall compare the supplied password with the stored User password. If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall decremented for each password mismatch when SECURITY UNLOCK and SECURITY ERASE UNIT commands shall be command aborted until a power-on reset or a hardware reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.

(27) Security Erase Prepare- F3h

Command Code: F3h

Feature Set: Security Mode feature set

Protocol

Non-data

Inputs

Table 72: Security erase prepare command for inputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F3h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 73: Security erase prepare command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

Error Outputs

The device shall return aborted if the device is in Frozen mode.

Table 74: Security erase prepare command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in Frozen mode. ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command prevents accidental loss of data on the device.

(28) Security Erase Unit- F4h

Command Code: F4h

Feature Set: Security Mode feature set

Protocol: PIO data-out.

Inputs

Table 75: Security erase unit command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F4h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 76: Security erase unit command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Table 77: Security erase unit command for error outputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one. This command shall be immediately preceded by a SECURITY ERASE PREPARE command.

Description

This command transfer 512 bytes of data from the host. Table12 defines the content of this information. If the password does not match the password previously saved by the device, the device shall reject the command with command aborted.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the device receives a SECURITY ERASE UNIT command without an immediately prior SECURITY

ERASE PREPARE command, the device shall command abort the SECURITY ERASE UNIT command.

When Normal Erase mode is specified, the SECURITY ERASE UNIT command shall write binary zeroes to all user data areas. The Enhanced Erase mode is optional. When Enhanced Erase Mode is specified, the device shall write predetermined data patterns to all user areas. In Enhanced Erase mode, all previously written user data shall be overwritten, including sectors that are no longer in use due to reallocation.

This command shall disable the device Lock mode, however, the Master password shall still be stored internally within the device and may be reactivated later a new User password is set.

Table 78: Security erase unit password information

Word	**Content**
0	Control Word Bit 0 Identifier 0=Compare User password 1= Compare Master password Bit 1 Erase mode 0=Normal Erase 1=Enhanced Erase Bit(15:2) Reserved
1-16	Password (32 Bytes)
17-255	Reserved

(29) Security Freeze Lock- F5h

Command Code: F5h

Feature Set: Security Mode feature set

Protocol: Non-data.

Inputs

Table 79: Security freeze lock for inputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	Na	Na	Na	Na	Na
Command	F5h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 80: Security freeze lock for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Table 81: Security freeze lock for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in locked mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

The SECURITY FREEZE LOCK command shall set the device to Frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen mode shall be disabled by power-off or hardware reset. If SECURITY FREEZE LOCK shall be issued when the device in Frozen mode, the command executes and the device shall remain in Frozen mode.

Command disabled by SECURITY FREEZE LOCK are:

- SECUIRTY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

(30) Security Disable Password- F6h

Command Code: F6h

Feature Set: Security Mode feature set

Protocol: PIO data-out.

Inputs

Table 82: Security disable password command for inputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F6h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 83: Security disable password command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

Error Outputs

The device shall return aborted if the device is in Locked mode, or device is in Frozen mode.

Table 84: Security disable password command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one. Device shall be in Unlocked mode.

Description

The SECURITY DISABLE PASSWORD command transfer 512 bytes of data from the host. Table 13 defines the content of this information. If the password selected by word 0 matches the password previously saved by the device, the device shall disable the Lock mode. This command shall not change the Master password. The Master password shall be reactivated when a User password if set.

Table 85: Security disable password command content

Word	Content
0	Control Word Bit 0 Identifier 0=Compare User password 1= Compare Master password Bit(15:1) Reserved
1-16	Password (32 Bytes)
17-255	Reserved

5.7. *SMART*

Individual SMART commands are identified by the value placed in the Feature register.

Table 86: SMART Feature register values

Value	Command
D0h	SMART Read Data
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS

5.7.1. SMART Read Data

Command Code: B0h with a Feature register value of D0h

Feature Set: Smart Feature Set

- Operation when the SMART feature set is implemented.

Protocol: PIO data-in

Inputs

Table 87: SMART command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							

LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register

DEV shall specify the selected device.

Normal Outputs

Table 88: SMART command for normal outputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

Prerequisites

DRDY set to one. SMART enabled.

Description

This command returns the Device SMART data structure to the host.

Table 89: SMART data structure

BYTE	**Description**
0-1	Revision code
2-361	Vendor specific
362	Off-line data collection status
363	Self-test execution status byte
364-365	Total time in seconds to complete off-line data collection activity
366	Vendor specific

367	Off-line data collection capability
368-369	SMART capability
370	Error logging capability *7-1 Reserved *0 1 = Device error logging supported
371	Vendor specific
372	Short self-test routine recommended polling time (in minutes)
373	Extended self-test routine recommended polling time (in minutes)
374	Conveyance self-test routine recommended polling time (in minutes)
375-385	Reserved
386-395	Firmware Version/Date Code
396-399	Reserved
400-406	'SMI2236'
407-511	Reserved
511	Checksum

5.7.2. SMART ENABLE OPERATIONS

Command Code

B0h with a Feature register value of D8h

Feature Set

Smart Feature Set

Protocol

Non-data

Inputs

Table 90: SMART Enable command for inputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Features	D8h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

Normal Outputs

Table 90: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

Prerequisites

DRDY set to one.

Description

This command enables access to all SMART capabilities within device.

5.7.3. SMART DISABLE OPERATIONS

Command Code: B0h with a Feature register value of D9h

Feature Set: Smart Feature Set

Protocol: Non-data

Inputs

Table 91: SMART DISABLE Command for inputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Features	D9h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

Normal Outputs

Table 92: SMART command for normal outputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

Prerequisites

DRDY set to one. SMART enabled.

Description

This command disables all SMART capabilities within device.

Appendix A. Ordering Information

1. Part Number List

Industrial CompactFlash Card – HERCULES-N Series (Plastic Frame-Kit)			
Product picture	**Grade**	**Commercial Grade (0°C ~ +70°C)**	**Industrial Grade (-40°C ~ +85°C)**
	**2GB**	**SPCFC002G-MNCTC-UF**	**WPCFC002G-MNITI-UF**
	4GB	**SPCFC004G-MNCTC-UF**	**WPCFC004G-MNITI-UF**
	8GB	**SPCFC008G-MNCTC-UF**	**WPCFC008G-MNITI-UF**
	16GB	**SPCFC016G-MNCTC-UF**	**WPCFC016G-MNITI-UF**
	32GB	**SPCFC032G-MNCTC-UF**	**WPCFC032G-MNITI-UF**
	64GB	**SPCFC064G-MNCTC-UF**	**WPCFC064G-MNITI-UF**
Industrial rugged metal CompactFlash Card – HERCULES-N Series			
Product picture	**Grade**	**Commercial Grade (0°C ~ +70°C)**	**Industrial Grade (-40°C ~ +85°C)**
	**2GB**	**SRCFC002G-MNCTC-UF**	**WRCFC002G-MNITI-UF**
	4GB	**SRCFC004G-MNCTC-UF**	**WRCFC004G-MNITI-UF**
	8GB	**SRCFC008G-MNCTC-UF**	**WRCFC008G-MNITI-UF**
	16GB	**SRCFC016G-MNCTC-UF**	**WRCFC016G-MNITI-UF**
	32GB	**SRCFC032G-MNCTC-UF**	**WRCFC032G-MNITI-UF**
	64GB	**SRCFC064G-MNCTC-UF**	**WRCFC064G-MNITI-UF**

2. Part Number Decoder

X1 X2 X3 X4 X5 X6 X7 X8 X9 – X11 X12 X13 X14 X15 – Z1 Z2 / C

Decoder Description

X1 : Grade

S : Standard Grade – operating temperature 0º C ~ 70 º C

W : Industrial Grade – operating temperature -40º C ~ +85 ºC

X2 : The material of case

P : Plastic frame

R : Rugged metal frame

X3 X4 X5 : Product category

CFC : CompactFlash Card

X6 X7 X8 X9 : Capacity

002G:	2GB	**016G:**	16GB
004G:	4GB	**032G:**	32GB
008G:	8GB	**064G:**	64GB

X11 : Controller

M : SMI (HERCULES-N Series)

X12 : Controller version

A, B, C, D…..

X13 : Controller Grade

C : Commercial grade

I : Industrial grade

X14 : Flash IC

T : Toshiba SLC Flash IC

X15 : Flash IC grade / Type

C : Commercial grade

I : Industrial grade

Z1 Z2 : Data transfer rate /CF disk type

PF : PIO-6 mode / fixed disk type

PR : PIO-6 mode / removable disk type

UF : Defaulted as UDMA-4 mode / fixed disk type

UR : UDMA-7 mode / removable disk type

AA : PIO/UDMA & fixed/removable disk type auto-detected

C : Reserved for specific requirement

C : Conformal-coating

Appendix B. Limited Warranty

APRO industrial CompactFlash (CF) Card HERCULES-N Series against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

Warranty Period:

- **SPCFCXXXG-MNCTC-UF** ***3 years***
- **WPCFCXXXG-MNITI-UF** ***5 years***

- **SRCFCXXXG-MNCTC-UF** ***3 years***
- **WRCFCXXXG-MNITI-UF** ***5 years***

The warranty period is able to extend. Please contact with APRO or Your APRO distributor for more information.