Tiger PCMCIA ATA Flash Card

Product Specification

Version 1.7

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Document Version

Version	Description	Date	Editor	Approved by
1.0	New issue	19,Dec.,2008	Amos Chung	Matika Wang
1.1	Fix capacity type	15,Feb.,2009	Matika Wang	David Lin
1.3	Fix error correction bits	18,Mar.,2009	Matika Wang	David Lin
1.4	Update	17,Dec.,2009	Amos Chung	Kent Liu
1.5	Modify performance	3,May,2010	Amos Chung	Kent Liu
1.6	Modify capacity to 64GB	23, Aug., 2010	Amos Chung	Kent Liu
1.7	Update vibration/shock data	28, July., 2011	Nelson Chen	Saber Lee

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Contents

1. Introduction

1.1 General Description

Pretec Tiger PCMCIA ATA Flash Card uses NAND-Type flash memory devices, which leads to its remarkable high performance and comes with capacities from 128 MB to 64GB unformatted.

Compliant with ISA (Industrial Standard Architecture) bus interface standard, the Tiger PCMCIA ATA Flash Card performs sequential read/write for each sector (512 bytes) count. It also conforms to PCMCIA specification and is designed with precision mechanics to enable host devices to read/write from the PCMCIA interface into flash media. It can operate with a 3.3V or 5V single power from the host side.

The card provides extraordinary memory medium for PC or any other electric equipment and digital still camera, and, in particular, Pretec Tiger PCMCIA ATA Flash Card has been approved through various compatibility tests to be used in numerous portable desktop, notebook computers and handheld PCs and auto PCs under industrial environment.

1.2 Features

- PC Card compliant
  - Conforms to CompactFlash standard
  - Compatible with PCMCIA ATA specification
  - Compatible with all PC Card Services and Socket Services
- PCMCIA ATA / IDE interface
  - ATA command set compatible
  - Support for 8-bit or 16-bit host data transfer
- Extremely rugged and reliable
  - Advanced defect block management
  - Support background erased operation
  - Dynamic Wear-Leveling
  - Power cycling test passed
- 3.3/5 Volt power supply, very low power consumption
  - ● Zero-power data retention, no batteries required
  - ● Internal self-diagnostic program operates at VCC power on
  - ● Auto sleep mode
- High reliability based on internal ECC (Error Correcting Code) function
  - ●Automatic on-the-fly, in-buffer error correction
  - ●Error Correction of 4 bits random error per sector
- 3 variations of mode access
  - ●Memory card mode
  - ●I/O card mode
  - ●True IDE mode
    - -PIO up to Mode 6
    - -UDMA up to mode 5

1.3 Part Number Definition

$X_1X_2\ X_3\ X_4X_5\ X_6\ X_7\ X_8$

Code	Definition	symbol	Description
X_1X_2	Card Type	PA	PCMCIA Type II
X_3	Solution	M	Tiger Series
$X_4X_5X_6$	Capacity	128	128MB
		256	256MB
		512	512MB
		01G	1GB
		02G	2GB
		04G	4GB
		06G	6GB
		08G	8GB
		16G	16GB
		32G	32GB
		64G	64GB
X_7	Temperature Range	C	Commercial Grade 0°C ~ 70°C
		L	Light Grade -20°C ~ +85°C
		H	Heavy Grade -40°C ~ +85°C
X_8	Housing	P	Plastic housing
		R	Metal housing

2. Product Specification

2.1 Operation and environment description

Operating Voltage	**DC Input Power**	5V ± 10%	
		3.3V ± 5%	
Typical Power Consumptions	5V	Read Mode: 84mA	
		Write Mode: 96mA	
		Standby Mode: 9.3mA	
	3.3V	Read Mode: 80mA	
		Write Mode: 75mA	
		Standby Mode: 1.1mA	
Environment Conditions	Operating Temperature	Extended Temp.	-20°C to +85°C
		Industrial Temp.	-40°C to +85°C
	Storage Temperature	Extended Temp.	-40°C to +90°C
		Industrial Temp.	-50°C to +90°C
	Humidity Operation	5% to 95% (Non-condensing)	
	Humidity Non-operation	5% to 95% (Non-condensing)	
	Shock Operation	Plastic Housing	50-G (Max)
		Material Housing	1500-G (Max)
	Shock Non-Operation	Plastic Housing	50-G (Max)
		Material Housing	1500-G (Max)
	Vibration Operation	20-G (Peak to peak to maximum)	
	Vibration Non-operation	20-G (Peak to peak to maximum)	
Operation System supported	DOS, Windows 98/ME/NT/2000/XP		

2.2 Physical description

Measures	Type II	L x W x H 85.6 x 54 x 5.0 (mm)
Storage Capacities	Capacity	128MB – 64GB
Performance	Data Transfer Rates	Read: 35 Mbytes/sec
		Write: 20 Mbytes/sec
Reliability	MTBF	3,000,000 hours
	Error Correction	More than 4 bit error correction per second read
	R/W Test	Test disk: 3,000,000 Read/Write cycles

3. Support Flash Media

3.1 Supported NAND Flash Type

3.1.1 Small block size of 16KB

Flash Capacity	128Mb	256Mb	512Mb
Operation Voltage	2.7V to 3.6V		

Unit: Bits

3.1.2 Large block size of 128KB

Flash Capacity	1Gb	2Gb	4Gb	8Gb
Operation Voltage	2.7V to 3.6V			

Unit: Bits

3.2 Logical Format Parameters (CHS)

Card Density[*1]	128MB	256MB	512MB	1GB	2GB	4GB
Cylinder	245	499	999	1,999	3,998	7,931
Heads	16	16	16	16	16	16
Sectors/Track[*2]	63	63	63	63	63	63
Total Sectors/Card[*3]	246,960	502,992	1,006,992	2,014,992	4,029,984	7,994,448
Capacity[*4]	127,688,704	256,712,704	514,760,704	1,030,848,512	2,061,991,936	4,083,580,928

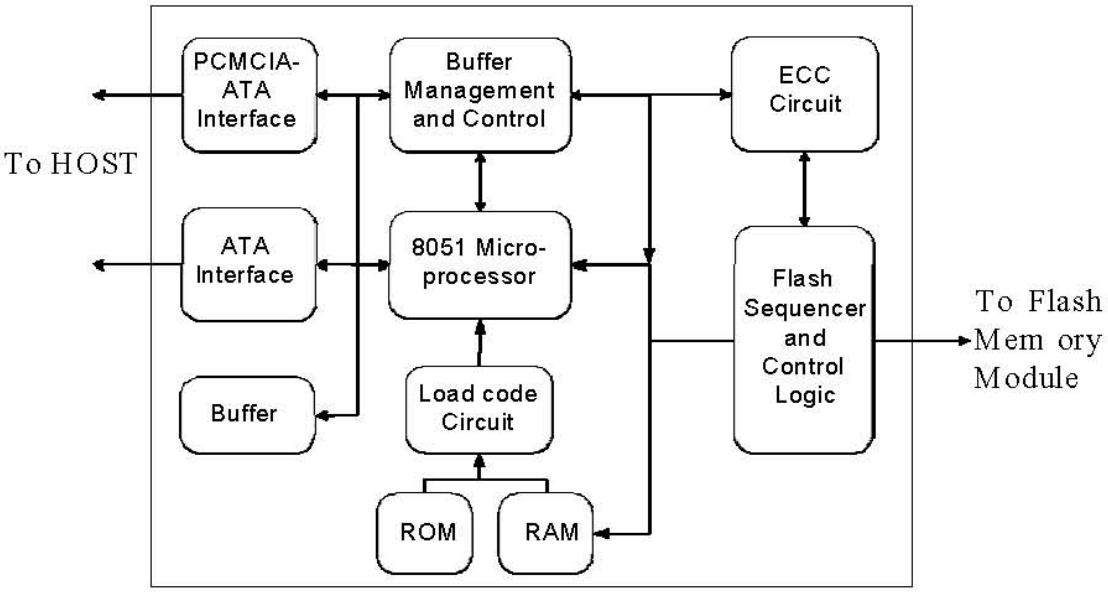
Card Density	6GB	8GB	16GB	32GB	64GB
Cylinder	11,995	15,863	16,383	16,383	16,383
Heads	16	16	16	16	16
Sectors/Track	63	63	63	63	63
Total Sectors/Card	12,090,960	15,989,904	16,514,064	16,514,064	16,514,064
Capacity	6,126,062,178	8,168,148,992	16,352,280,576	32,704,561,152	65,409,122,304

Unit: Bytes

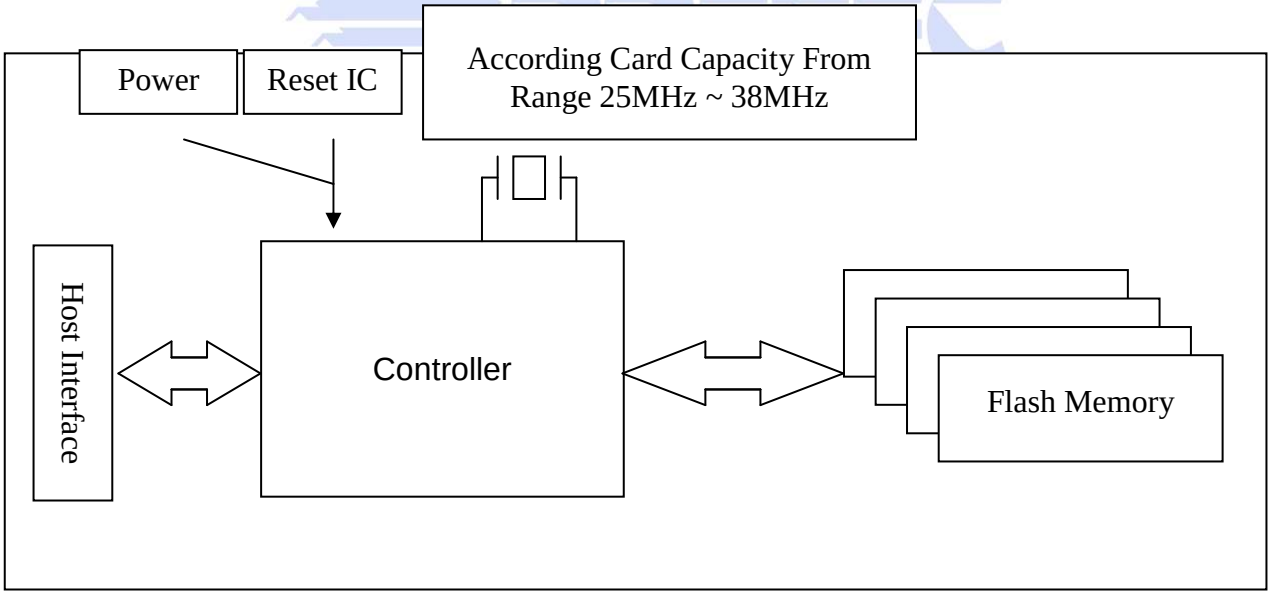
Notes:
[*]1. It's the logical address capacity including the area which is used for file system.
[*]2. Total tracks = number of head x number of cylinder.
[*]3. Total sector/Card = sector/track x number of head x number of cylinder.
[*]4. Those are general unformatted capacity of all cards.

4. Block Diagram

4.1 Controller Architecture



4.2 Flash Card Architecture



5. Specification and Features

5.1 Electrical Specification

5.1.1 Recommended Operating Conditions

Operating Conditions	Min.	Typ.	Max.
I/O DC Supply Voltage (5V)	4.5 V	5 V	5.5 V
I/O DC Supply Voltage (3.3V)	3.0 V	3.3 V	3.6 V
Temperature	-40℃	25℃	85℃

5.1.2 DC Electrical Characteristics for 5 Volts Operation

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	High level output voltage	I_{OH}=4.8mA	V_{CC} – 0.8	-	-	V
V_{OL}	Low level output voltage	I_{OL}=4.8mA	-	-	0.4	V
V_{CC}	Power supply	-	4.5	5.0	5.5	V
T_{OPR}	Operating temperature	-	-40	-	85	℃
V_{IL}	Input low voltage	CMOS	-	-	0.8	V
V_{IH}	Input high voltage	CMOS	2.0	-	-	V

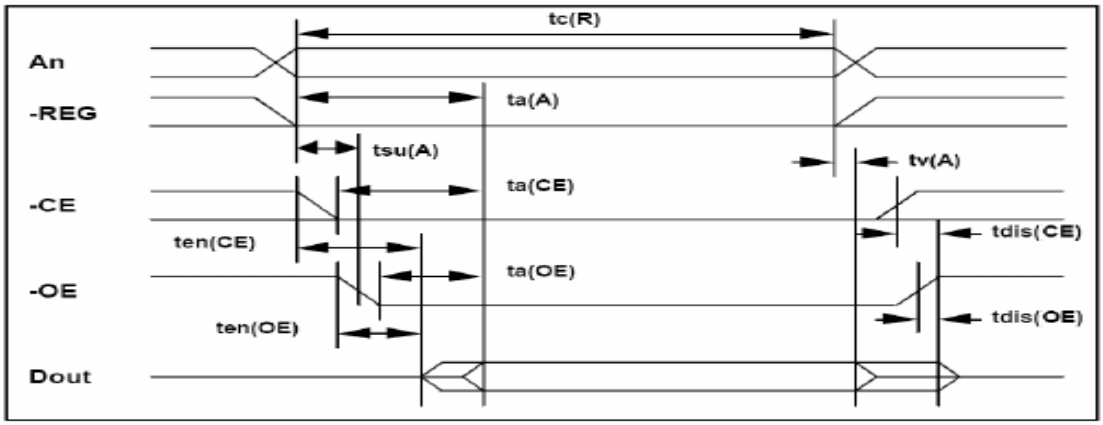
5.1.3 DC Electrical Characteristics for 3.3 Volts Operation

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	High level output voltage	I_{OH}=2~16mA	2.4	-	-	V
V_{OL}	Low level output voltage	I_{OL}=2~16mA	-	-	0.4	V
V_{CC}	Power supply	-	3.0	3.3	3.6	V
T_{OPR}	Operating temperature	-	-40	-	85	℃
V_{IL}	Input low voltage	CMOS	-	-	0.8	V
V_{IH}	Input high voltage	CMOS	2.0	-	-	V

5.1.4 Attribute Memory Read Timing Specification

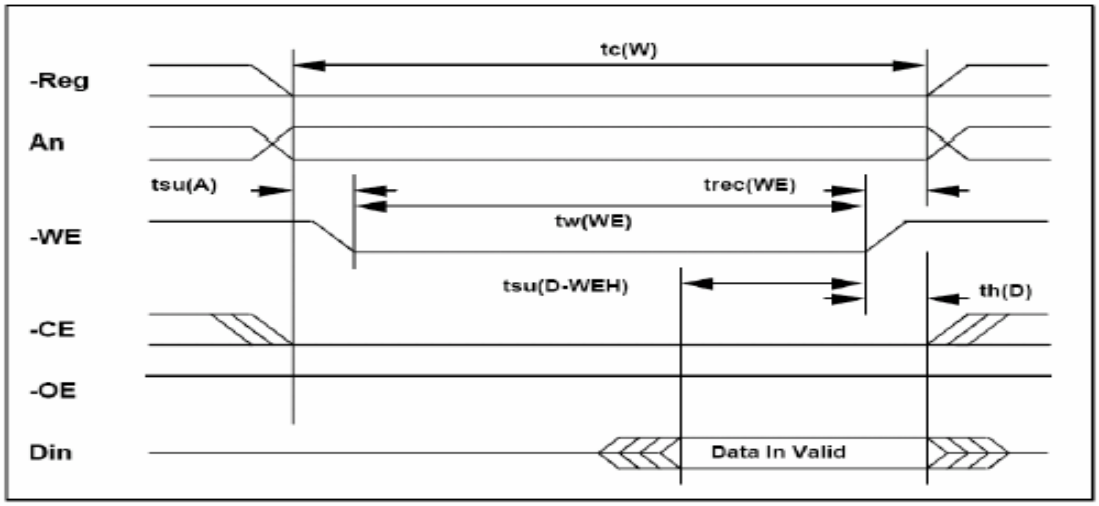
Item	Symbol	IEEE Symbol	Min.(ns)	Max. (ns)
Read Cycle Time	tc(R)	tAVAV	300	-
Address Cycle Time	ta(A)	tAVQV	-	300
Card Enable Access Time	ta(CE)	tELQV	-	300
Output Enable Access Time	ta(OE)	tGLQV	-	150

Item	Symbol	IEEE Symbol	Min.(ns)	Max. (ns)
Output Disable Time from CE	tdis(CE)	tEHQZ	-	100
Output Disable Time from OE	tdis(OE)	tGHQZ	-	100
Address Setup Time	tsu (A)	tAVGL	30	-
Output Enable Time from CE	ten(CE)	tELQNZ	5	-
Output Enable Time from OE	ten(OE)	tGLQNZ	5	-
Data Valid from Address Change	tv(A)	tAXQX	0	-



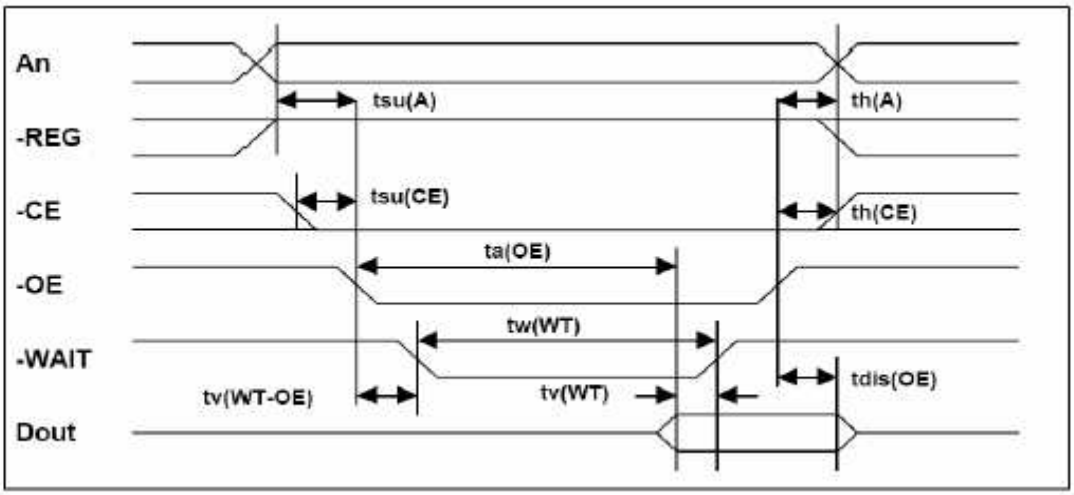
5.1.5 Configuration Register (Attribute Memory) Write Timing Specification

Item	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Write Cycle Time	tc(W)	tAVAV	250	-
Write Pulse Width	tw(WE)	tWLWH	150	-
Address Setup Time	tsu(A)	tAVWL	30	-
Write Recovery Time	trec(WE)	tWMAX	30	-
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	-
Data Hold Time	th(D)	tWMDX	30	-



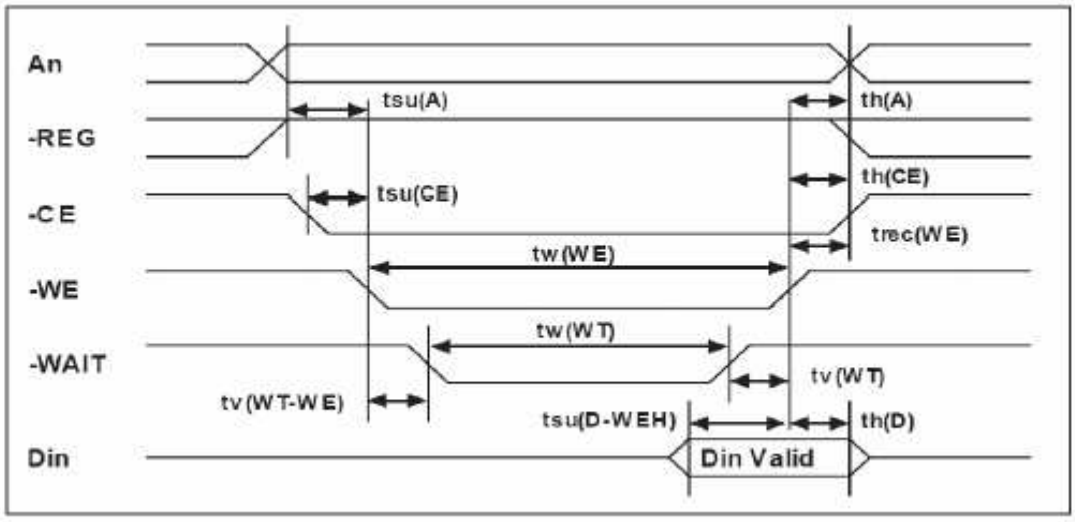
5.1.6 Common Memory Read Timing Specification

Item	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Output Enable Access Time	ta(OE)	tGLQV	-	125
Output Disable Time from OE	tdis(OE)	tGHQZ	-	100
Address Setup Time	tsu(A)	tAVGL	30	-
Address Hold Time	th(A)	tGHAX	20	-
CE Setup before OE	tsu(CE)	tELGL	0	-
CE Hold following OE	th(CE)	tGHEH	20	-
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV	-	35
Data Setup for Wait Release	tv(WT)	tQVWTH	-	0
Wait Width Time	tw(WT)	tWTLWTH	-	350 (3000 for CF+)



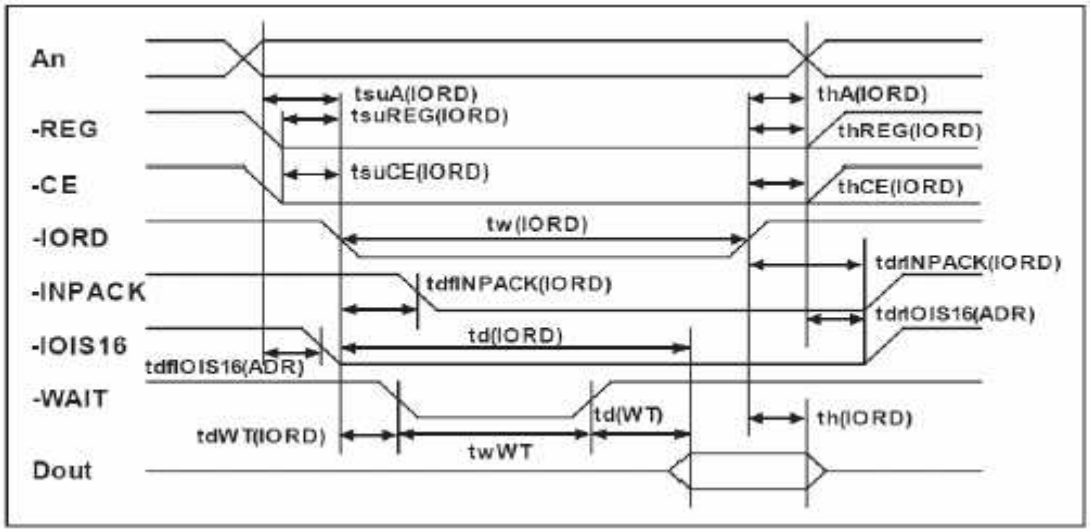
5.1.7 Common Memory Write Timing Specification

Item	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Data Setup before WE	tsu(D-WEH)	tDVWH	80	-
Data Hold following WE	th(D)	tWMDX	30	-
WE Pulse Width	tw(WE)	tWLWH	150	-
Address Setup Time	tsu(A)	tAVWL	30	-
CE Setup before WE	tsu(CE)	tELWL	0	-
Write Recovery Time	trec(WE)	tWMAX	30	-
Address Hold Time	th(A)	tGHAX	20	-
CE Hold following WE	th(CE)	tGHEH	20	-
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV	-	35
WE High from Wait Release	tv(WT)	tWTHWH	0	-
Wait Width Time	tw (WT)	tWTLWTH	-	350 (3000 for CF+)



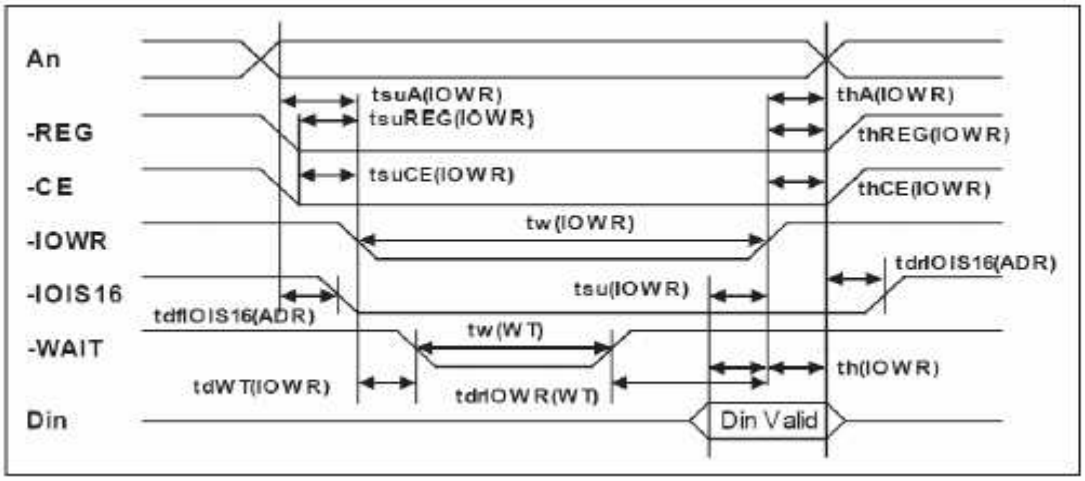
5.1.8 I/O Input (Read) Timing Specification

Item	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Data Delay after IORD	td(IORD)	tIGLQV	-	100
Data Hold following IORD	th(IORD)	tIGHQX	0	-
IORD Width Time	tw(IORD)	tIGLIGH	165	-
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	-
Address Hold following IORD	thA(IORD)	tIGHAX	20	-
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	-
CE Hold following IORD	thCE(IORD)	tIGHEH	20	-
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5	-
REG Hold following IORD	thREG(IORD)	tIGHRGH	0	-
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45
INPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH	-	45
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL	-	35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH	-	35
Wait Delay Falling from IORD	tdWT(IORD)	tIGLWTL	-	35
Data Delay from Wait Rising	td(WT)	tWTHQV	-	0
Wait Width Time	tw(WT)	tWTLWTH	-	350 (3000 for CF+)



5.1.9 I/O Input (Write) Timing Specification

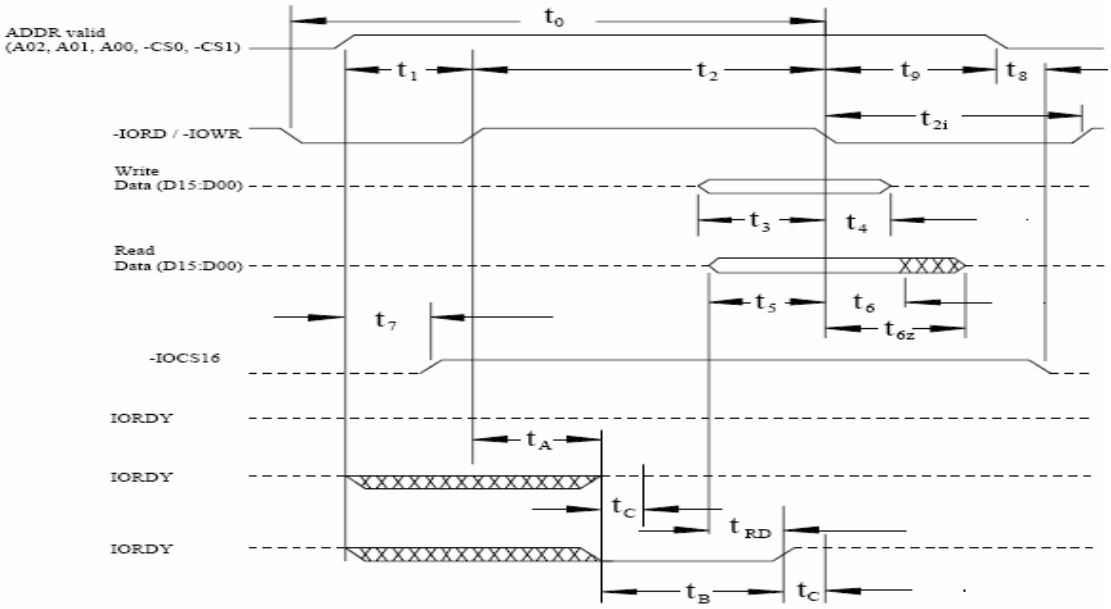
Item	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	-
Data Hold following IOWR	th(IOWR)	tIWHDX	30	-
IOWR Width Time	tw(IOWR)	tIWLIWH	165	-
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	-
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	-
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	-
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	-
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5	-
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0	-
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL	-	35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH	-	35
Wait Delay Falling from IOWR	tdWT(IOWR)	tIWLWTL	-	35
IOWR high from Wait high	tdrIOWR(WT)	tWTJIWH	0	-
Wait Width Time	tw(WT)	tWTLWTH	-	350



5.1.10 True IDE Mode PIO (Read/Write) Timing Specification

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Note
t0	Cycle time (min)	600	383	240	180	120	100	80	
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55	
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	25	20	
t3	-IOWR data setup (min)	60	45	30	30	20	20	15	
t4	-IOWR data hold (min)	30	20	15	10	10	5	5	
t5	-IORD data setup (min)	50	35	20	20	20	15	10	
t6	-IORD data hold (min)	5	5	5	5	5	5	5	
t6Z	-IORD data tristate (max)	30	30	30	30	30	20	20	
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	na	na	
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na	na	
tC	IORDY assertion to release (max)	5	5	5	5	5	na	na	

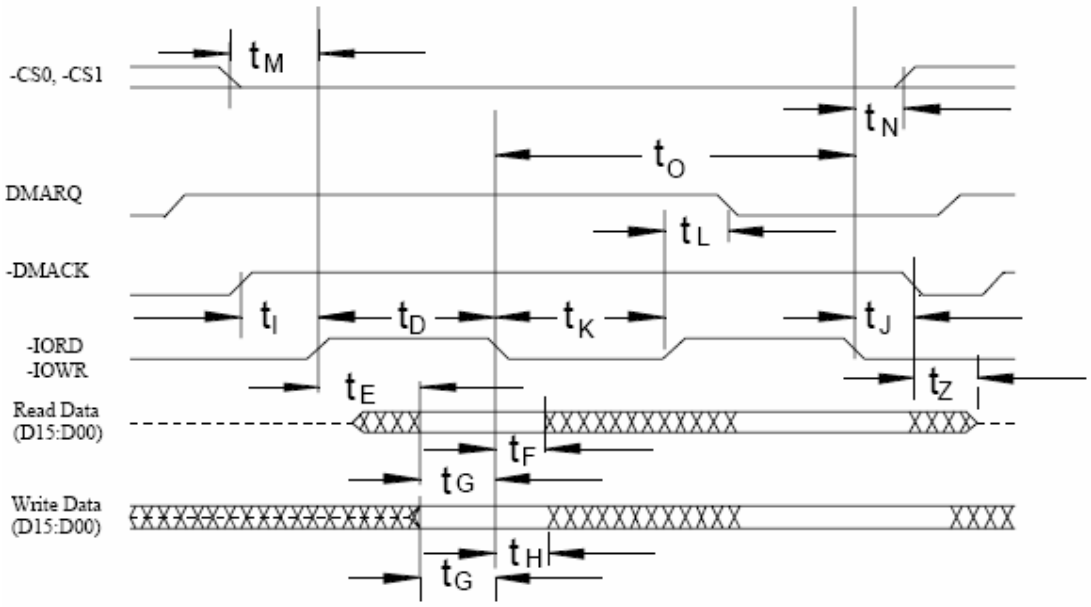
5.1.11 True IDE PIO Mode Timing Diagram



5.1.12 True IDE Multiword DMA Mode I/O (Read/Write) Timing Specification

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)
t_O	Cycle time (min)	480	150	120	100	80
t_D	-IORD / -IOWR asserted width (min)	215	80	70	65	55
t_E	-IORD data access (max)	150	60	50	50	45
t_F	-IORD data hold (min)	5	5	5	5	5
t_G	-IORD/-IOWR data setup (min)	100	30	20	15	10
t_H	-IOWR data hold (min)	20	15	10	5	5
t_I	DMACK to –IORD/-IOWR setup (min)	0	0	0	0	0
t_J	-IORD / -IOWR to -DMACK hold (min)	20	5	5	5	5
t_{KR}	-IORD negated width (min)	50	50	25	25	20
t_{KW}	-IOWR negated width (min)	215	50	25	25	20
t_{LR}	-IORD to DMARQ delay (max)	120	40	35	35	35
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	35	35
t_M	CS(1:0) valid to –IORD / -IOWR	50	30	25	10	5
t_N	CS(1:0) hold	15	10	10	10	10
t_Z	-DMACK	20	25	25	25	25

5.1.13 True IDE Multiword DMA Mode Read/Write Timing Diagram



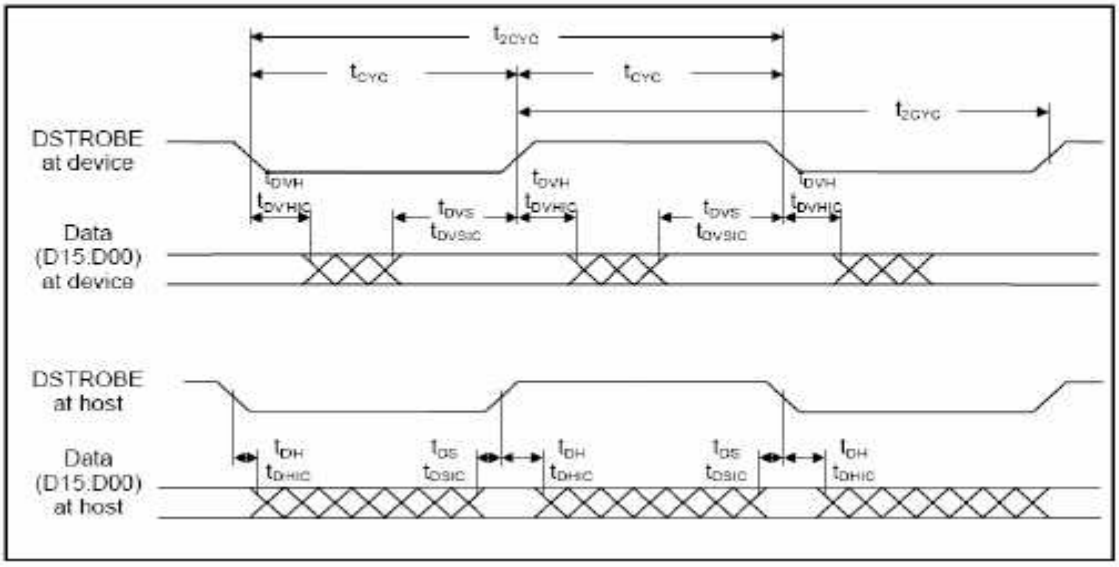
5.1.14 Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0 (in ns)		UDMA Mode 1 (in ns)		UDMA Mode 2 (in ns)		UDMA Mode 3 (in ns)		UDMA Mode 4 (in ns)		UDMA Mode 5 (in ns)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
$t_{2CYCTYP}$	240		160		120		90		60		40	
t_{CYC}	112		73		54		39		25		16.8	
t_{2CYC}	230		153		115		86		57		38	
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0	
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6	
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8	
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8	
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0	
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0	
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0	
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0	
t_{ZFS}	0		0		0		0		0		35	
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25	
t_{FS}		230		200		170		130		120		90
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75
t_{MLI}	20		20		20		20		20		20	
t_{UI}	0		0		0		0		0		0	
t_{AZ}		10		10		10		10		10		10
t_{ZAH}	20		20		20		20		20		20	
t_{ZAD}	0		0		0		0		0		0	
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50
t_{RFS}		75		70		60		60		60		50
t_{RP}	160		125		100		100		100		85	
t_{IORDYZ}		20		20		20		20		20		20
t_{ZIORDY}	0		0		0		0		0		0	
t_{ACK}	20		20		20		20		20		20	
t_{SS}	50		50		50		50		50		50	

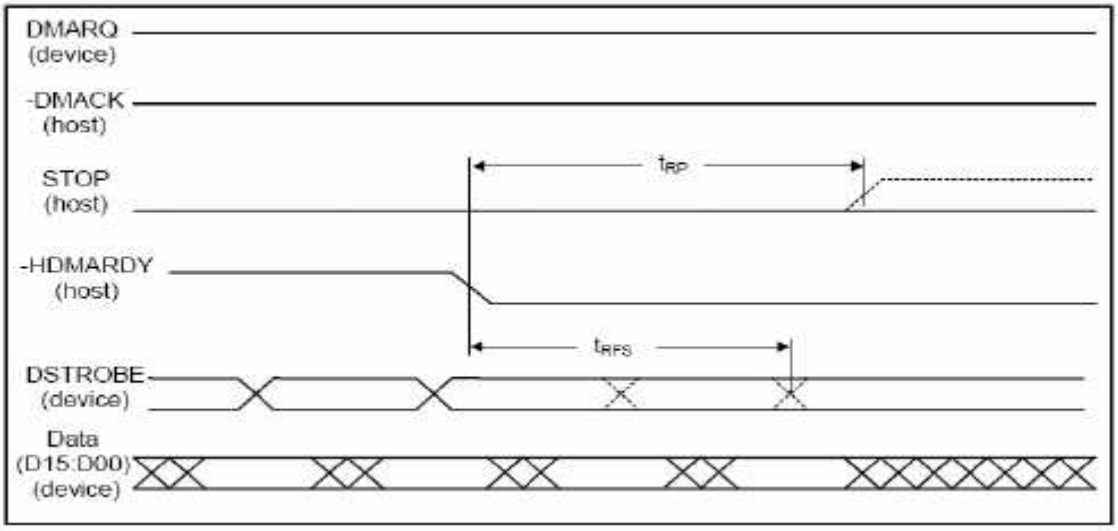
5.1.15 Ultra DMA Data Burst Timing Descriptions

Name	Comment
$t_{2CYCTYP}$	Typical sustained average two cycle time
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)
t_{CS}	CRC word setup time at device
t_{CH}	CRC word hold time device
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
t_{LI}	Limited interlock time
t_{MLI}	Interlock time with minimum
t_{UI}	Unlimited interlock time
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)
t_{ZAH}	Minimum delay time required for output
t_{ZAD}	drivers to assert or negate (from released)
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)
t_{IORDYZ}	Maximum time before releasing IORDY
t_{ZIORDY}	Minimum time before driving IORDY
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

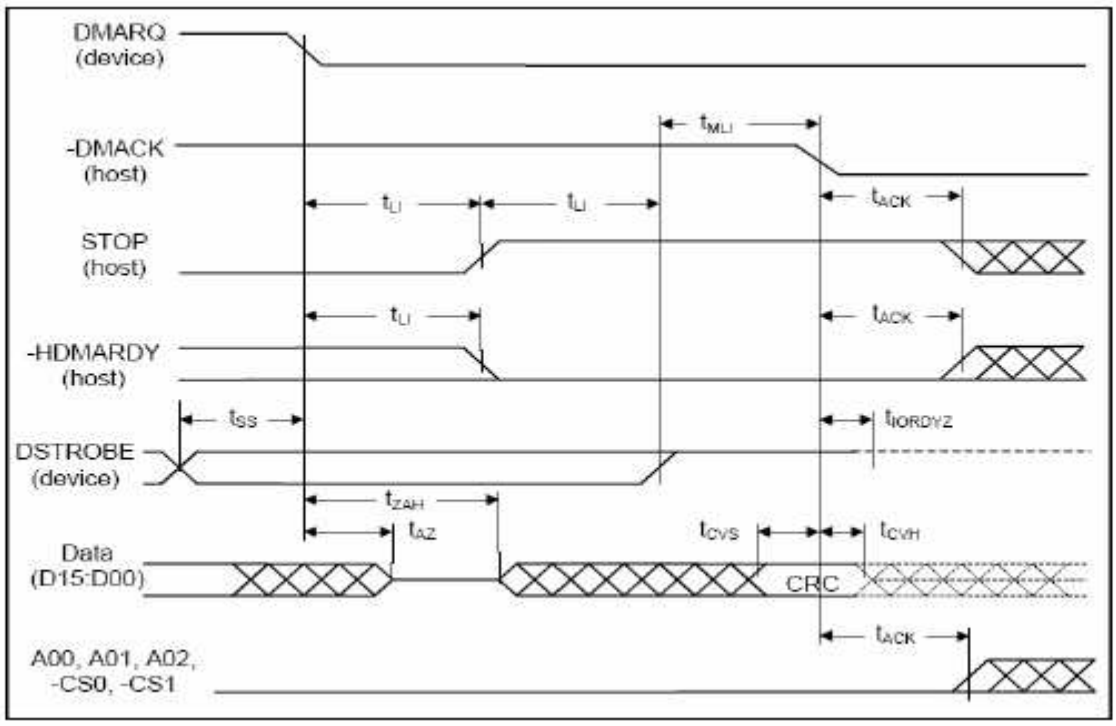
5.1.16 Sustained Ultra DMA Data-In Burst Timing



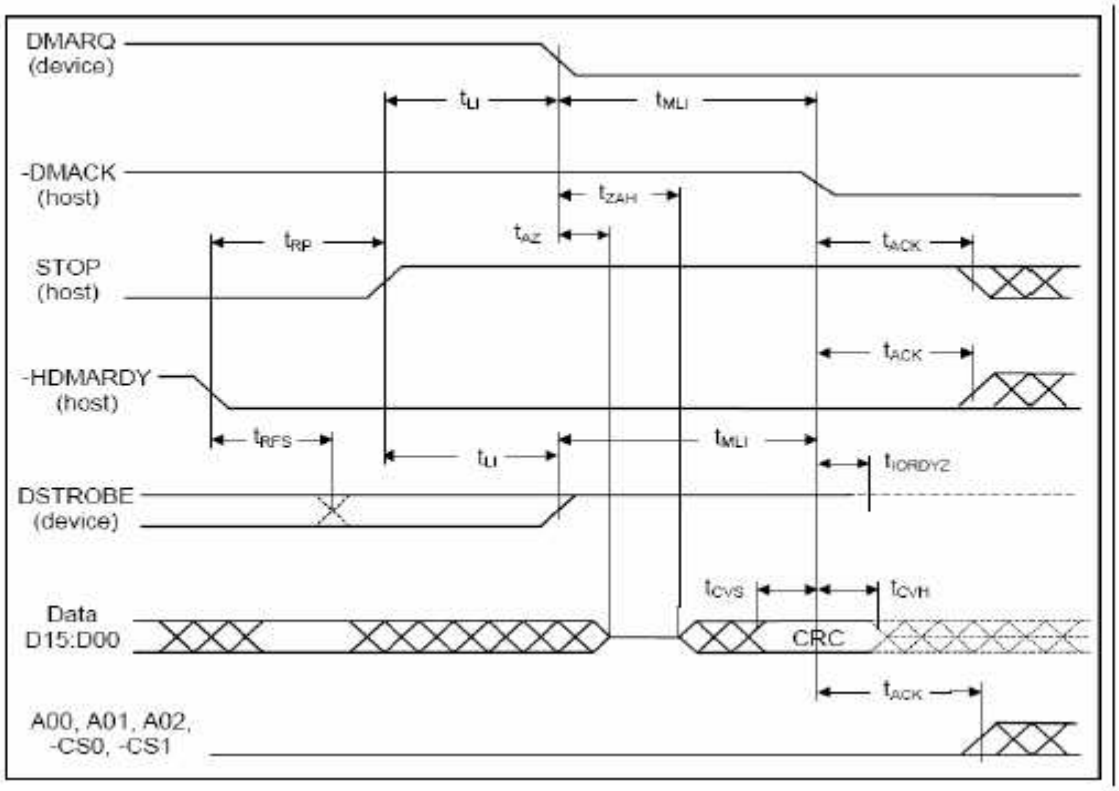
5.1.17 Ultra DMA Data-In Burst Host Pause Timing



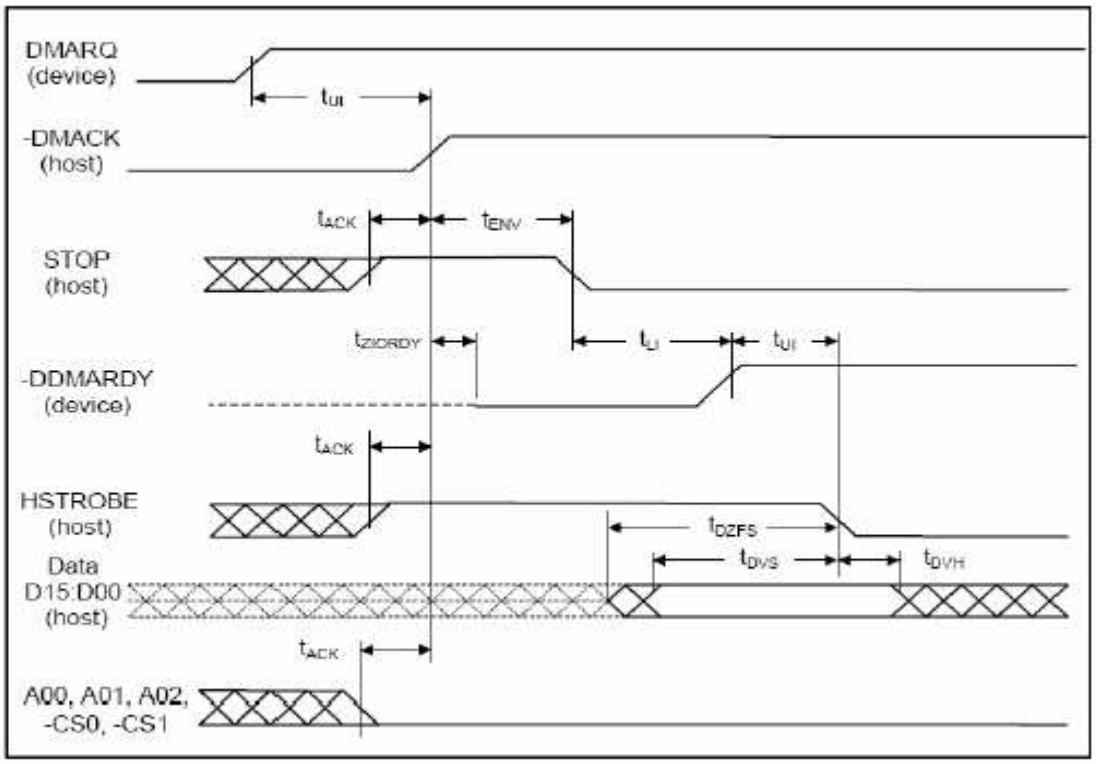
5.1.18 Ultra DMA Data-In Burst Device Termination Timing



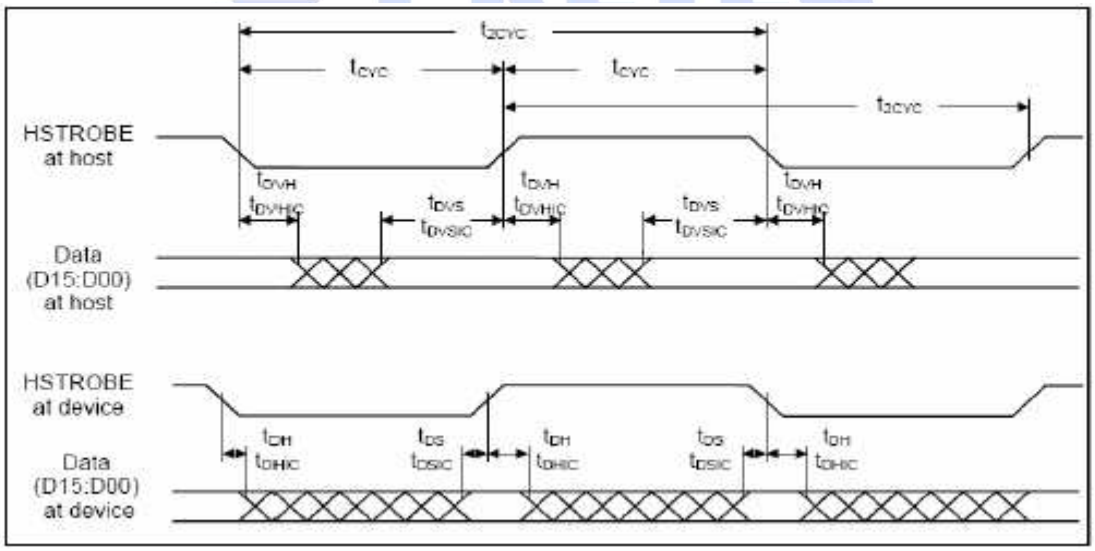
5.1.19 Ultra DMA Data-In Burst Host Termination Timing



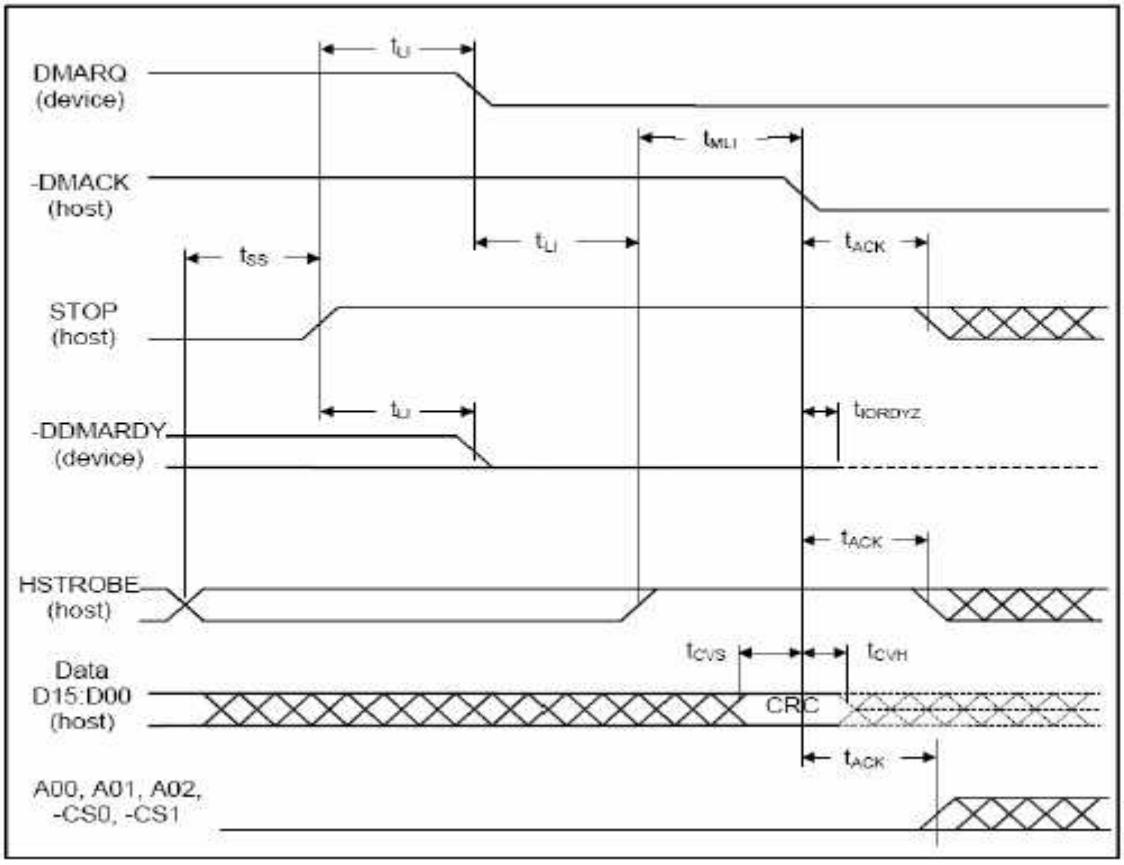
5.1.20 Ultra DMA Data-Out Burst Host Initiation Timing



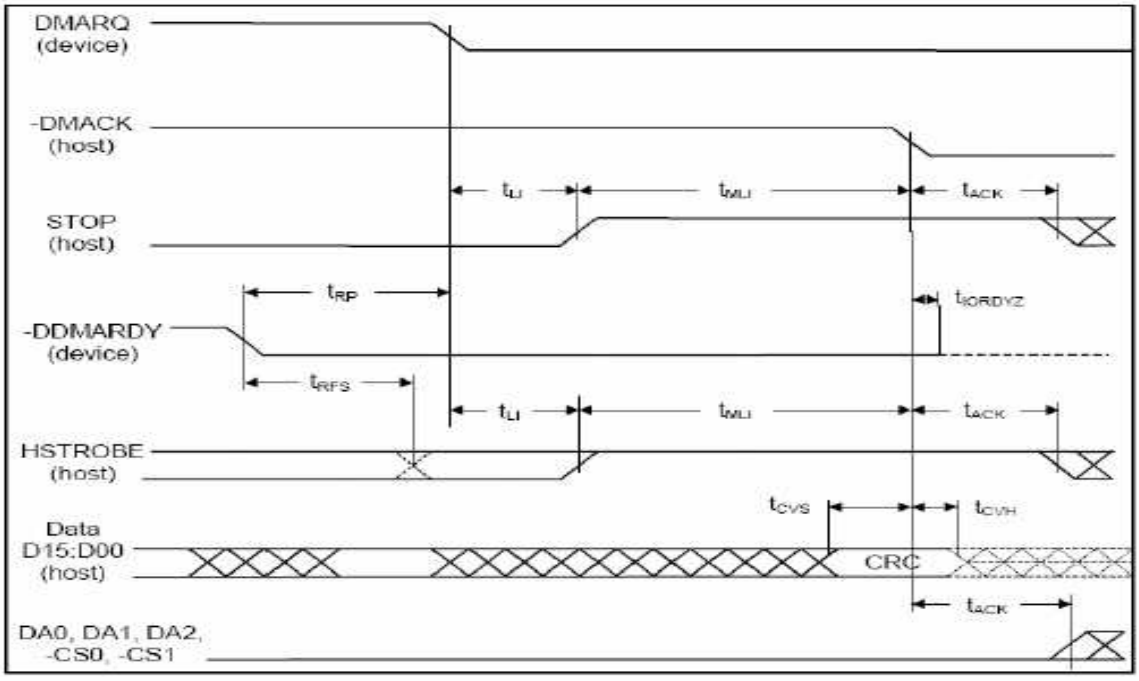
5.1.21 Sustained Ultra DMA Data-Out Burst Timing



5.1.22 Ultra DMA Data-Out Burst Host Termination Timing



5.1.23 Ultra DMA Data-Out Burst Device Termination Timing



5.2 Power Management

5.2.1 Normal Mode

The host can reduce the power consumption of the card by changing its status with the following Power Command.

Sleep mode consumes the lowest power. Response time for the card to change from sleep mode to the active state is about 30 ms or less.

Standby mode, the response time is about 5ms or less. This is due to the interface of the card that accepts the command although can't access the media immediately

Idle mode, the card can respond and access the media immediately. The card needs longer time in this mode than in its active mode in order to active several circuits that were not used in the active mode.

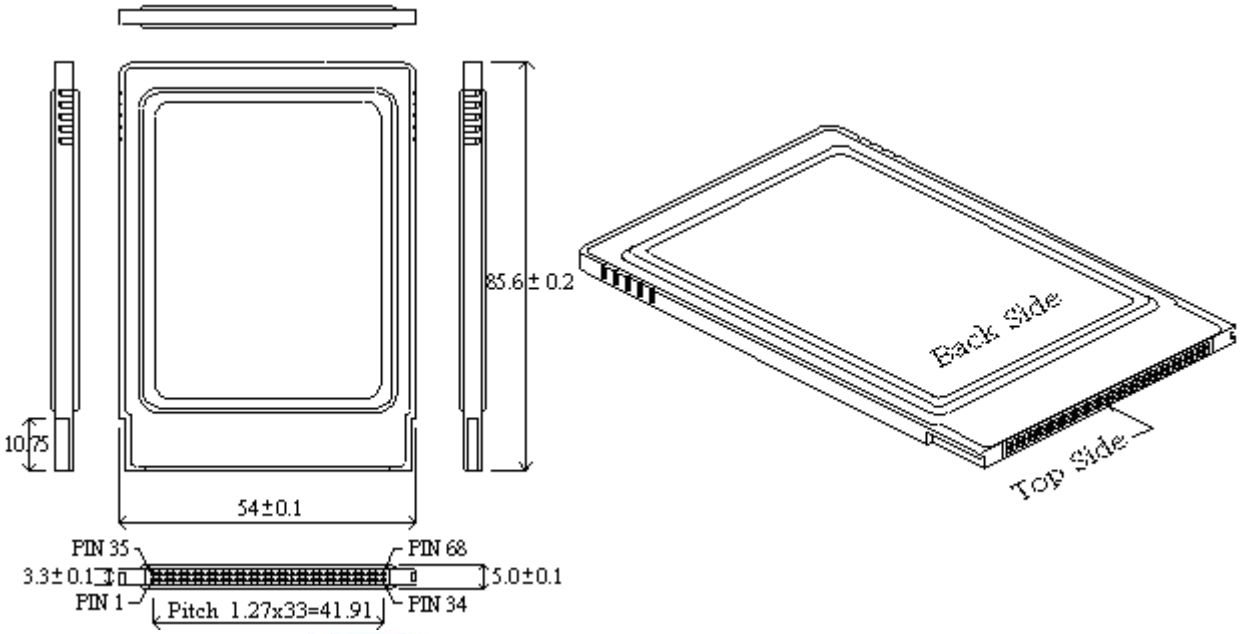
Active mode, the card can respond and access the media immediately and the commands are processed with no delay.

5.2.2 Power Down Mode

This card can set itself into Power Down Mode. To enable this mode, it is needed to use the Information Change command, which is a vender unique command. The advantage of using this mode is the ability to move automatically into Sleep mode after command completion.

6. Physical Specification

6.1 PCMCIA ATA (Type II)



7. Pin Assignment

7.1 PCMCIA ATA

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
No.	Pin Name	I/O	No.	Pin Name	I/O	No.	Pin Name	I/O
1	GND	-	1	GND		1	GND	-
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	#CE1	I	7	#CE1	I	7	#CS1	I
8	A10	I	8	A10	I	8	A10	I
9	#OE	I	9	#OE	I	9	#ATASEL	I
10	----	-	10	----	-	10	----	-
11	A09	I	11	A09	I	11	A09	I
12	A08	I	12	A08	I	12	A08	I
13	----	-	13	----	-	13	----	-
14	----	-	14	----	-	14	----	-
15	#WE	I	15	#WE	I	15	#WE	I
16	RDY/#BSY	O	16	#IREQ	O	16	INTRQ	O
17	VCC	-	17	VCC	-	17	VCC	-
18	----	-	18	----	-	18	----	-
19	----	-	19	----	-	19	----	-
20	----	-	20	----	-	20	----	-
21	----	-	21	----	-	21	----	-
22	A07	I	22	A07	I	22	A07	I
23	A06	I	23	A06	I	23	A06	I
24	A05	I	24	A05	I	24	A05	I
25	A04	I	25	A04	I	25	A04	I
26	A03	I	26	A03	I	26	A03	I
27	A02	I	27	A02	I	27	A02	I
28	A01	I	28	A01	I	28	A01	I
29	A00	I	29	A00	I	29	A00	I
30	D00	I/O	30	D00	I/O	30	D00	I/O
31	D01	I/O	31	D01	I/O	31	D01	I/O
32	D02	I/O	32	D02	I/O	32	D02	I/O
33	WP	O	33	#IOIS16	O	33	#IOIS16	O
34	GND	-	34	GND	-	34	GND	-
35	GND	-	35	GND	-	35	GND	-
36	#CD1	O	36	#CD1	O	36	#CD1	O
37	D11	I/O	37	D11	I/O	37	D11	I/O
38	D12	I/O	38	D12	I/O	38	D12	I/O
39	D13	I/O	39	D13	I/O	39	D13	I/O
40	D14	I/O	40	D14	I/O	40	D14	I/O
41	D15	I/O	41	D15	I/O	41	D15	I/O
42	#CE2	I	42	#CE2	I	42	#CS2	I
43	#VS1	O	43	#VS1	O	43	#VS1	O
44	RESERVED	-	44	#IORD	I	44	#IORD	I
45	RESERVED	-	45	#IOWR	I	45	#IOWR	I
46	----	-	46	----	-	46	----	-
47	----	-	47	----	-	47	----	-
48	----	-	48	----	-	48	----	-
49	----	-	49	----	-	49	----	-

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
50	----	-	50	----	-	50	----	-
51	VCC	-	51	VCC	-	51	VCC	-
52	----	-	52	----	-	52	----	-
53	----	-	53	----	-	53	----	-
54	----	-	54	----	-	54	----	-
55	----	-	55	----	-	55	----	-
56	#CSEL	I	56	#CSEL	I	56	#CSEL	I
57	#VS2	O	57	#VS2	O	57	#VS2	O
58	RESET	I	58	RESET	I	58	#RESET	I
59	#WAIT	O	59	#WAIT	O	59	IORDY	O
60	RESERVED	-	60	#INPACK	O	60	#INPACK	O
61	#REG	I	61	#REG	I	61	#REG	I
62	BVD2	I/O	62	#SPKR	I/O	62	#DASP	I/O
63	BVD1	I/O	63	#STSCHG	I/O	63	#PDIAG	I/O
64	D08	I/O	64	D08	I/O	64	D08	I/O
65	D09	I/O	65	D09	I/O	65	D09	I/O
66	D10	I/O	66	D10	I/O	66	D10	I/O
67	#CD2	O	67	#CD2	O	67	#CD2	O
68	GND	-	68	GND	-	68	GND	-

7.2 Signal Description

Signal Name	Description	IO	Pin
A0-A10 (PC Card Memory Mode)	These address lines along with the #REG signal are used to select the following: The I/O port address registers within the adapter.	I	8,11,12, 22,23,24, 25,26,27, 28,29
A0-A10 (PC Card I/O Mode)	This signal is the same as the PC Card Memory Mode signal.		
A0-A2 (True IDE Mode)	In True IDE Mode only A0-A2 are used to select the one of eight registers in the ATA Task File, the other address lines should be grounded.		27,28,29
BVD1 (PC Card Memory Mode)	This signal is asserted high as the BVD1 signal since a battery is not used with this adapter.	I/O	63
#STSCHG (PC Card I/O Mode)	This signal is asserted low to alert the host to changes in the RDY/#BSY and Write Protect states, while the I/O interface is configured. It is controlled by the Card Configure and Status Register.		
#PDIAG (True IDE Mode)	In the True IDE Mode, this I/O is the Pass Diagnostic signal in the Master/Slave handshake protocol.		
BVD2 (PC Card Memory Mode)	This signal is always driven to a high state in Memory Mode since a battery is not required for this adapter.	I/O	62
#SPKR (PC Card I/O Mode)	This signal is always driven to a high state in I/O Mode since this adapter does not support the audio function.		

Signal Name	Description	IO	Pin
#DASP (True IDE Mode)	In the True IDE Mode, this I/O is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.	-	-
#CD1, #CD2 (PC Card Memory Mode)	These Card Detect pins are connected to ground on this adapter.	O	36,67
#CD1, #CD2 (PC Card I/O Mode)	They are used to determine if the adapter is fully inserted into the socket.		
#CD1, #CD2 (True IDE Mode)			
#CE1,#CE2 (PC Card Memory Mode)	These signals are used both to select the adapter and to indicate to the adapter whether a byte or a word operation is being performed. #CE2 always accesses the odd byte of the word. #CE1 accesses the even byte or the odd byte of the word depending on A0 and #CE2.	I	7,42
#CE1,#CE2 (PC Card I/O Mode)		-	-
#CS1,#CS2 (True IDE Mode)	In the True IDE Mode, #CS1 is the chip select for the Task File Registers while #CS2 is used to select the Alternate Status and the Device Control Register.		
#CSEL (PC Card Memory Mode)	This signal is not used for this mode.	I	56
#CSEL (PC Card I/O Mode)	This signal is not used of this mode.		
#CSEL (True IDE Mode)	This internally pulled up signal is used to configure this adapter as a Master or a Slave. When this pin is grounded, this adapter is Master. When this pin is open, this adapter is Slave.		
D0-D15 (PC Card Memory Mode)	These lines carry the Data, Commands and Status between the host and controller. D00 is the LSB of the even byte of the word. D08 is the LSB of the odd byte of the word.	I/O	41,40,39, 38,37,66, 65,64,6,5, 4,3,2,32, 31,30
D0-D15 (PC Card I/O Mode)			
D0-D15 (True IDE Mode)	In True IDE Mode, all Task File operations occur in the byte mode on the low order D00-D07 while all data transfers are 16 bits using D00-D15.		
GND (PC Card Memory Mode)	Ground.	-	1,34,35,68
GND (PC Card I/O Mode)			
GND (True IDE Mode)			

Signal Name	Description	IO	Pin
RESERVED (PC Card Memory Mode)	This signal is not used in this mode.	O	60
#INPACK (PC Card I/O Mode)	The Input Acknowledge signal is asserted by the adapter when the adapter is selected and responding to an I/O read cycle at the address that is on the address bus.		
#INPACK (True IDE Mode)	In the True IDE mode, this signal is not used.		
RESERVED (PC Card Memory Mode)	This signal is not used in this mode.	I	44
#IORD (PC Card I/O Mode)	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the adapter when the adapter is configured to use the I/O interface.		
#IORD (True IDE Mode)	In the True IDE mode, the signal is the same as the I/O Mode.		
RESERVED (PC Card Memory Mode)	This signal is not used in this mode.	I	45
#IOWR (PC Card I/O Mode)	The I/O Write strobe is used to clock I/O data on the Data bus into the adapter controller registers when the adapter is configured to use the I/O interface.		
#IOWR (True IDE Mode)	In the True IDE Mode, this signal is the same as the I/O mode.		
#OE (PC Card Memory Mode)	This is an Output Enable Strobe generated by the host interface. It is used to read data from the adapter in Memory Mode and to read CIS and configuration registers.	I	9
#OE (PC Card I/O Mode)	In I/O Mode, this signal is used to read the CIS and configuration registers.		
#ATASEL (True IDE Mode)	To enable True IDE Mode, this signal should be grounded by the host.		
RDY/#BSY (PC Card Memory Mode)	In the Memory Mode, this signal is set high when adapter is ready to accept a new data transfer operation and held low when the card is busy.	O	16
#IREQ (PC Card I/O Mode)	I/O Operation. After the adapter has been configured for I/O Mode, this signal is used as Interrupt Request.		
INTRQ (True IDE Mode)	In the True IDE Mode, this signal is the active high Interrupt Request to the host.		

Signal Name	Description	IO	Pin
#REG (PC Card Memory Mode)	This signal is used during Memory Cycle to distinguish between Common Memory and Attribute Memory accesses. High for Common	I	61
#REG (PC Card I/O Mode)	Memory and Low for Attribute Memory. This signal muse be low during I/O Cycles when the I/O address is on the Bus.		
#REG (True IDE Mode)	In the True IDE Mode, this signal is not used and should be connected to VCC by the host.		
RESET (PC Card Memory Mode) RESET (PC Card I/O Mode)	When the signal is high, the signal Resets the adapter.	I	58
#RESET (True IDE Mode)	In the True IDE Mode, the signal is the active low hardware reset from the host.		
VCC (PC Card Memory Mode)	5V , 3.3V	-	17,51
VCC (PC Card I/O Mode)			
VCC (True IDE Mode)			
#VS1,#VS2 (PC Card Memory Mode)	Voltage Sense Signals.	O	43,57
#VS1,#VS2 (PC Card I/O Mode)			
#VS1,#VS2 (True IDE Mode)			
#WAIT (PC Card Memory Mode)	This signal is driven low by the adapter to notice the host to delay completion of the a memory of I/O cycle that is in progress.	O	59
#WAIT (PC Card I/O Mode)			
IORDY (True IDE Mode)	In the True IDE Mode, this signal may be used as IORDY.		
#WE (PC Card Memory Mode)	This signal is driven by the host and used for generating memory write cycle to the registers of the adapter when the adapter is configured in the Memory mode.	I	15
#WE (PC Card I/O Mode)	In I/O mode, this signal is used for writing the configuration registers.		
#WE (True IDE Mode)	In the True IDE Mode, this signal is not used and should be connected to VCC by the host.		
WP (PC Card Memory Mode)	Memory Mode, the adapter doesn't have a write protect switch. This signal is held low.	O	33

Signal Name	Description	IO	Pin
#IOIS16 (PC Card I/O Mode)	I/O Mode, A low signal indicates that a 16 bits or odd byte only operation can be performed by the addressed port.	-	-
#IOIS16 (True IDE Mode)	In the True IDE Mode, this signal is asserted low when this device is expecting a word data transfer cycle.		

8. CIS and Functions Configuration Registers

This card supports four Configuration Registers for the purpose of the configuration and observation of this card. These registers can be used in memory and I/O card mode. In True IDE mode, these register can not be used.

8.1 Configuration Option Register (200H)

This register is used for the configuration of the card and allows issuing software reset through this register.

<Reset value = 00H>

D7	D6	D5	D4	D3	D2	D1	D0
SRESET	LevlREQ	INDEX					
R/W	R/W	R/W					

Index Those bits are used for selecting an operation mode of the card as follows. When Power on, Card Hard Reset and Soft Rest, this data is “000000” for the Memory mode card interface recognition.

LevlREQ This bit sets to “0” when pulse mode interrupt is selected, and sets to “1” when level mode interrupt is selected.

SRESET Setting this bit to “1”, places the card in the reset state (Card Hard Reset).This operation is equal to Hard Reset, except this bit is not cleared. Card configuration status is reset and the card internal initialized operation starts when Card Hard Reset is executed, so next access to the card should be the same sequence as the power on sequence.

Index Bits Assignment

INDEX bits						Task File register address	Mapping mode
5	4	3	2	1	0		
0	0	0	0	0	0	OH to FH, 400h to 7FFH	Memory mode
0	0	0	0	0	1	xx0H to xxFH	Independent I/O mode
0	0	0	0	1	0	1F0H to 1F7H, 3F6H to 3F7H	Primary I/O mapped
0	0	0	0	1	1	170H to 177H, 376H to 377H	Secondary I/O mapped

8.2 Card Configuration and Status Register (Address 202H)

This register is used for observing the card state.

<Reset value = 00H>

D7	D6	D5	D4	D3	D2	D1	D0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0
R	R/W	R/W	---	---	R/W	R	---

INTR INTERRUPT: When set, indicates that the #IREQ pin is low. When clear, indicates that the #IREQ pin is high. This bit state is available whether I/O

card interface has been configured or not. If interrupts are disabled by the #IEN bit in the Device Control Register, this bit is zero.

PWD — POWER DOWN: When set, the card enters sleep state (Power Down mode). When clear, the card transfers to idle state (active mode).

IOIS8 — I/O IS 8 bit: When set, indicates that the data bus width of the host is 8 bits (D0-D7). When clear, indicates that the data bus width of the host is 16 bits (D0-D15).

SIGCHG — SIGNAL CHGED: This bit is set and reset by the host to enable and disable a state-change signal from the Status Register, the CHANGED bit control pin 46 and the CHANGED Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (#STSCHG) signal will be held high while thie card is configured for I/O.

CHGED — Indicated that one or both of the pin Replacement Register (204H) Crdy, or CWProt bits are set to one (1). When changed bit is set, #STSCHG pin 46 is held low if the SIGCHG bit is a one (1) and the card is configured for I/O interface.

8.3 Pin Replacement Register (Address 204H)

This register is used for providing the signal state of #IREQ signal when the card configured I/O card interface.

<Reset value = 0CH>

D7	D6	D5	D4	D3	D2	D1	D0
0	0	CRDY	0	1	1	RRDY	RWProt
---		R/W		---		R/W	0

RWProt — READ WRITE PROTECT: this bit indicates the write protect status. When set, indicates write protect. When cleared indicates write is enable.

PRDY — This bit is used to determine the internal state of the RDY/BSY signal. This bit may be used to determine the state of the Ready/Busy as this pin has been reallocated for use as interrupt Request on an I/O card.

CEProt — This bit is set to one (1) when RWProt changes state. This bit may be written by the host.

CRDY — CARD READY: This bit is set to one (1) when the READY bit changes state. This bit may be written by the host.

8.4 Socket and Copy Register (Address 206H)

This register is used for identification of the card from other cards. The host can read and write this register. The host shall set this register before the card's Configuration Option Register is set.

<Read, Reset value = 00H>

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	DRV#	0	0	0	0
---	---	---	R/W	---	---	---	---

DRV# DRIVE NUMBER: This bit is set by the host and compared to the DRV bit (D4), in the ATA Drive/Head Register. In this way, host can perform the card's master/slave organization.

8.5 Card Information Structure (CIS)

The CIS is attribute information of the card and its characteristics, which includes information about the type of card and the manufacturer. The CIS is allocated in the beginning of the attribute memory, between addresses 0 and 255. The data is allocated in the even addresses only. The Host uses these registers to initialize and configure the card.

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
000H	01H	CISTPL_JEDEC	Device info tuple	Tuple code
002H	04H	TPL_LINK	Link length is 4 byte	Link to next tuple
004H	02H	Device type W Device speed P S	Device type= DH: I/O device WPS=1:No WP Device Speed=7: ext speed	Device type, WPS, speed
006H	79H	EXT Speed Speed Mantissa exponent	400 ns if not wait	Extended speed
008H	01H	1x 2k units	2k byte of address space	Device size
00AH	FFH	List end marker	End of device	End marker
00CH	1CH	CISTP_DEVICE_OC	Other conditions device info tuple	Tuple code
00EH	04H	TPL_LINK	Link length 4 bytes	Link to next tuple
010H	02H	EXT Reserved Vcc MWAIT	3V, wait is not used	Other conditions info field
012H	DBH	Device type W Device speed P S	Device type= DH: I/O device WPS=1:No WP Device Speed=1:250 ns	Device type, WPS, speed
014H	01H	1x 2k units	2k byte of address space	Device size
016H	FFH	List end marker	End of device	END marker
018H	18H	CISTPL_JEDEC_C	JEDEC ID common memory	Tuple code
01AH	02H	TPL_LINK	Link length is 2 bytes	Link to next tuple
01CH	DFH	PCMCIA's manufacturer's JEDEC ID Code	Manufacturer's ID code	JEDEC ID of PC Card ATA
01EH	01H	PCMCIA JEDEC device code	2nd byte of JEDEC ID	-
020H	20H	CISTPL_MANFID	Manufacturer's ID code	Tuple code
022H	04H	TPL_LINK	Link length is 4 bytes	Link to next tuple
024H	45H	Low byte of PCMCIA manufacturer's code	manufacturer's ID	Low byte of manufacturer's ID code
026H	00H	High byte of PCMCIA manufacturer's code	Code of 0 because other byte is JEDEC 1 byte manufacturer's ID	High byte of manufacturer's ID code
028H	01H	Low byte of product code	For PC CARD ATA	Low byte of product code
02AH	04H	High byte of product code		High byte of product code
02CH	15H	CISTPL_VERS_1	Level 1 version/product info	Tuple code

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
02EH	1AH	TPL_LINK	Link length is 26 bytes	Link to next tuple
030H	04H	TPPLV1_MAJOR	PCMCIA2.0/JEIDA4.1	Major version
032H	01H	TPPLV1_MINOR	PCMCIA2.0/JEIDA4.1	Minor version
034H	43H	-	'C'	Info string 1
036H	46H	-	'F'	-
038H	20H	-	' '	-
03AH	43H	-	'C'	-
03CH	61H	-	'a'	-
03EH	72H	-	'r'	-
040H	64H	-	'd'	-
042H	00H	-	Null terminator	-
044H	43H	-	'C'	Info string 2
046H	46H	-	'F'	-
048H	41H	-	'A'	-
04AH	20H	-	' '	-
04CH	XXH	-	'X'	According for card capacity.
04EH	XXH	-	'X'	-
050H	XXH	-	'X'	-
052H	XXH	-	'X'	-
054H	4DH	-	'M'	-
056H	42H	-	'B'	-
058H	20H	-	' '	-
05AH	43H	-	'C'	-
05CH	4BH	-	'K'	-
05EH	52H	-	'S'	-
060H	00H	-	Null terminator	-
062H	FFH	List end marker	End of device	END marker
064H	21H	CISTPL_FUNCID	Function ID tuple	Tuple code
066H	02H	TPL_LINK	Link length is 2 bytes	Link to next tuple
068H	04H	TPLFID_FUNCTION=04H	Disk function, may be silicon, may be removable	PC card function code
06AH	01H	Reserved R P	R=0: No BIOS ROM P=1: Configure card at power on	System initialization byte
06CH	22H	CISTPL_FUNCE	Function extension tuple	Tuple code
06EH	02H	TPL_LINK	Link length 2 bytes	Link to next tuple
070H	01H	Disk function extension tuple type	Disk interface type	Extension tuple type for disk

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
072H	01H	Disk interface type	PC card ATA interface	Interface type
074H	22H	CISTPL_FUNCE	Function extension tuple	Tuple code
076H	03H	TPL_LINK	Link length is 3 bytes	Link to next tuple
078H	02H	Disk function extension tuple type	Single drive	Extension tuple type for disk
07AH	0CH	Reserve D U S V	No Vpp< Silicon, single drive V=0: No Vpp required S=1: Silicon U=1: Unique serial# D=0: Single drive on card	Basic ATA option Parameter byte 2
07CH	0FH	R I E N P3 P2 P1 P0	P0: Sleep mode supported P1: Standby mode supported P2: Idle mode supported P3: Drive auto power control N: Some config excludes 3X7 E: Index bit is emulated I: Twin IOIS 16# datd reg only R: Reserved	Basic ATA option parameter byte 2
07EH	1AH	CISTPL_CONFIG	Configuration tuple	Tuple code
080H	05H	TPL_LINK	Link length is 5 bytes	Link to next tuple
082H	01H	RFS RMS RAS	RFS: Reserved RMS: TPCC_RMSK size-1=0 RAS:TPCC_RADR size-1=1 1 byte register mask 2 b2 byte config base address	Size of fields byte TPCC_SZ
084H	03H	TPCC_LAST	Entry with config index of 03H is final entry in table	Last entry of config registers
086H	00H	TPCC_RADR(LSB)	Configuration registers are located at 200H in REG space	Location of config registers
088H	02H	TPCC_RADAR(MSB)	-	-
08AH	0FH	Reserved S P C I	I: Configuration index C: configuration and status P: Pin replacement S: Socket and copy	Configuration registers present mask TPCC_RMSK
08CH	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
08EH	08H	TPL_LINK	Link length is 8 bytes	Link to next tuple
090H	C0H	I D Configuration Index	Memory mapped I/O configuration I=1: Interface byte follows D=1: Default entry Configuration index=0	Configuration table index byte TPCE_INDX
092H	40H	W R P B Interface type	W=0: Wait not used R=1: Ready active P=0: WP not used B=0: BVD1and BVD2 not used IF type=0: Memory interface	Interface description field TPCE_IF

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
094H	A1H	M MS IR IO T P	M=1: Misc info present MS=01: Memory space info single 2-byte length IR=0: No interrupt info present IO=0: No I/O port info present T=0: No toming info present P=1: Vcc only info	Feature selection TPCE_FS
096H	01H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for Vcc
098H	55H	X Mantissa Exponent	Nominal voltage=5V	Vcc nominal value
09AH	08H	Length in 256 bytes pages (LSB)	Length of memory space is 2 KB	Memory space description structures (TPCE_MS)
09CH	00H	Length in 256 bytes pages (MSB)	-	-
09EH	20H	X R P RO A T	X=0: No more misc fields R: Reserved P=1: Power down supported RO=0: Not read only mode A=0: Audio not supported T=0: Single drive	Miscellaneous features field TPCE_MI
0A0H	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
0A2H	06H	TPL_LINK	Link length is 6 bytes	Link to next tuple
0A4H	00H	I D Configuration Index	Memory mapped I/O configuration I=0: No interface byte D=0: No Default entry Configuration index=0	Configuration table index TPCE_INDX
0A6H	01H	M MS IR IO T P	M=0: No misc info MS=00: No memory space inflo IO=0: No I/O port info present T=0:No timing info present P=0: Vcc only info	Feature selection byte TPCE_FS
0A8H	21H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for Vcc
0AAH	B5H	X Mantissa Exponent	Nominal Voltage=3.0V	Vcc nominal value
0ACH	1EH	X Extension	+0.3 V	Extension byte

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
0AEH	4DH	X Mantissa Exponent	Max average current over 10 msec is 45 mA	Max. average current
0B0H	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
0B2H	0AH	TPL_LINK	Link length is 10 bytes	Link to next tuple
0B4H	C1H	I D Configuration INDEX	Contiguous I/O mapped ATA registers configuration I=1: Interface byte follows D=1: Default entry Configuration index=1	Configuration table index byte TPCE_INDX
0B6H	41H	W R P B Interface type	W=0: Wait not used R=1: Ready active P=0: WP not used B=0: BVS1 and BVS2 not used IF type=1: I/O interface	Interface description field TPCE_IF
0B8H	99H	M MS IR IO T P	M=1: Misc info present MS=00: No memory space info IR=1: Interrupt info present IO=1: I/O port info present T=0: No timing info present P=1:Vcc only info	Feature selection byte TPCE_FS
0BAH	01H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for Vcc
0BCH	55H	X Mantissa Exponent	Nominal Voltage=5V	Vcc nominal value
0BEH	64H	R S E IO AddrLine	S=1: 16-bit hosts supported E=1: 8-bit hosts supported IO AddrLine:4 lines decoded	I/O space description field TPCE_IO
0C0H	F0H	S P L M V B I N	S=1: Share logic active P=1: Pulse mode IRQ supported L=1: Level mode IRQ supported M=1: Bit mask of IRQ present V=0: No vender unique IRQ B=0: No bus error IRQ I=0: No IO check IRQ N=0: No NMI	Interrupt request description structure TPCE_IR
0C2H	FFH	IRQ IR IR IR IR IR OR IRQ0 7 Q Q Q Q Q Q 6 5 4 3 2 1	IRQ level to be routed 0 to 15 recommended	Mask extension byte 1 TPCE_IR
0C4H	FFH	IRQ IR IR IR IR IR OR IRQ8 15 Q Q Q Q Q Q 14 13 12 11 10 9	Recommended routing to any “normal, maskable” IRQ	Mask extension byte 2 TPCE_IR

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
0C6H	20H	X R P RO A T	X=0: Nomore misc fields R: reserved P=1: Power down supported RO=0: Not read only mode A=0: Audi not supported T=0: Single drive	Miscellaneous features field TPCE_MI
Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
0C8H	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
0CAH	06H	TPL_LINK	Link length is 6 bytes	Link to next tuple
0CCH	01H	I D Configuration index	Contiguous I/O mapped ATA registers configuration I=0: No Interface byte D=0: No Default entry Configuration index=1	Configuration table index byte TPCE_INDX
0CEH	01H	M MS IR IO T P	M=0: No Misc info present MS=00: No memory space info IR=0: No Interrupt info present IO=0: No I/O port info present T=0: No timing info present P=1:Vcc only info	Feature selection byte TPCE_FS
0D0H	21H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for Vcc
0D2H	B5H	X Mantissa Exponent	Nominal voltage = 3.0V	Vcc nominal value
0D4H	1EH	X Extension	+0.3V	Extension byte
0D6H	4DH	X Mantissa Exponent	Max. average current over 10 msec is 45mA	Max. average current
0D8H	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
0DAH	0FH	TPL_LINK	Link length is 15 bytes	Link to next tuple
0DCH	C2H	I D Configuration index	Contiguous I/O mapped ATA registers configuration I=1: Interface byte follows D=1: Default entry follows Configuration index=2	Configuration table index byte TPCE_INDX
0E0H	41H	W R P B Interface type	W=0: Wait not used R=1: Ready active P=0: WP not used B=0: BVS1 and BVS2 not used IF type=1: I/O interface	Interface description field TPCE_IF

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
0E2H	99H	M MS IR IO T P	M=1: Misc info present MS=00: No memory space info IR=1: Interrupt info present IO=1: I/O port info present T=0: No timing info present P=1:Vcc only info	Feature selection byte TPCE_FS
0E4H	01H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for Vcc
0E6H	55H	X Mantissa Exponent	Nominal Voltage=5V	Vcc nominal value
0E8H	EAH	R S E IO AddrLine	R=1: Range follows S=1:16-bit hosts supported E=1: 8-bit hosts supported IO AddrLines: 10 lines decoded	I/O space description field TPCE_IO
0EAH	61H	-	-	-
0ECH	FOH	-	1st I/O base address(LSB)	1st I/O range address
0EEH	01H	-	1st I/O base address(MSB)	
0F0H	07H	-	1st I/O length-1	1st I/O range length
0F2H	F6H	-	2nd I/O base address(LSB)	2nd I/O range address
0F4H	03H	-	2nd I/O base address(MSB)	-
0F6H	01H	-	2nd I/O length-1	2nd I/O range length
0F8H	EEH	S P L M IRQ level	S=1: Share logic active P=1: Pulse mode IRQ supported L=1: Level mode IRQ supported M=0: Bit mask of IRQ present IRQ level is ORQ 14	Interrupt request description structure TPCE_IR
0FAH	20H	X R P RO A T	X=0: Nomore misc fields R: reserved P=1: Power down supported RO=0: Not read only mode A=0: Audi not supported T=0: Single drive	Miscellaneous features field TPCE_MI
0FEH	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
0FCH	06H	TPL_LINK	Link length is 15 bytes	Link to next tuple
100H	02H	I D Configuration index	ATA primary I/O mapped configuration I=0: No Interface byte D=0: No Default entry Configuration index=2	Configuration table index byte TPCE_INDX

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
102H	01H	M MS IR IO T P	M=0: No Misc info MS=00: No memory space info IR=0: No Interrupt info present IO=0: No I/O port info present T=0: No timing info present P=1: Vcc only info	Feature selection byte TPCE_FS
104H	21H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for Vcc
106H	B5H	X Mantissa Exponent	Nominal voltage =3.0V	Vcc nominal value
108H	1EH	X Extension	+0.3V	Extension byte
10AH	4DH	X Mantissa Exponent	Max average current over 10 msec is 45mA	Max. average current
10CH	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
10EH	0FH	TPL_LINK	Link length is 15 bytes	Link to next tuple
110H	C3H	I D Configuration index	ATA secondary I/O mapped configuration I=1: Interface byte follow D=1: Default entry Configuration index=3	Configuration table index byte TPCE_INDX
112H	99H	M MS IR IO T P	M=1: Misc info present MS=00: No memory space info IR=1: Interrupt info present IO=1: I/O port info present T=0: No timing info present P=1:Vcc only info	Feature selection byte TPCE_FS
114H	41H	W R P B Interface type	W=0: Wait not used R=1: Ready active P=0: WP not used B=0: BVS1 and BVS2 not used IF type=1: I/O interface	Interface description field TPCE_IF
116H	01H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max. voltage info LV: Min. voltage info NV: Nominal voltage info	Power parameters for Vcc
118H	55H	X Mantissa Exponent	Nominal Voltage=5V	Vcc nominal value

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
11AH	EAH	R S E IO AddrLine	R=1: Range follows S=1:16-bit hosts supported E=1: 8-bit hosts supported IO Addr Lines: 10 lines decoded	I/O space description field TPCE_IO
11CH	61H	LS AS N range	LS=1: Size of lengths is 1 byte AS=2: Size of address is 2 bytes N Range=1: Address range-1	I/O range format description
11EH	70H	-	1st I/O base address(LSB)	1st I/O range address
120H	01H	-	1st I/O base address(MSB)	-
122H	07H	-	1st I/O length-1	1st I/O range length
124H	76H	-	2nd I/O base address(LSB)	2nd I/O range address
126H	03H	-	2nd I/O base address(MSB)	-
128H	01H	-	2nd I/O length-1	2nd I/O range length
12CH	EEH	S P L M IRQ level	S=1: Share logic active P=1: Pulse mode IRQ supported L=1: Level mode IRQ supported M=0: Bit mask of IRQ present IRQ level is ORQ 14	Interrupt request description structure TPCE_IR
12AH	20H	X R P RO A T	X=0: Nomore misc fields R: reserved P=1: Power down supported RO=0: Not read only mode A=0: Audi not supported T=0: Single drive	Miscellaneous features field TPCE_MI
12EH	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
130H	06H	TPL_LINK	Link length is 6 bytes	Link to next tuple
132H	03H	I D Configuration index	ATA secondary I/O mapped configuration I=0: No Interface byte D=0: No Default entry Configuration index=3	Configuration table index byte TPCE_INDX
134H	01H	M MS IR IO T P	M=0: No Misc info MS=00: No memory space info IR=0: No Interrupt info present IO=0: No I/O port info present T=0: No timing info present P=1: Vcc only info	Feature selection byte TPCE_FS

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
136H	21H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for Vcc
138H	1EH	X Extension	+0.3V	Extension byte
140H	B5H	X Mantissa Exponent	Nominal voltage =3.0V	Vcc nominal value
142H	4DH	X Mantissa Exponent	Max average current over 10 msec is 45mA	Max. average current
144H	14H	CISTPL_NO_LINK	No link control tuple	Tuple code
146H	00H	-	Link is 0 bytes	Link to next tuple
148H	FFH	CISTPL_END	End of tuple	Tuple code

9. ATA Specific Register Definitions

As we described the adapter provides several kinds of addressing modes, Memory mode, I/O mode, and True IDE mode. Below are described the procedures access for accessing each mode the Task File registers.

9.1 Memory Mapped Addressing

#REG	Offset	A10	A4 – A9	A3	A2	A1	A0	#OE = "0"	#WE = "0"
1	0H	0	X	0	0	0	0	Even read data	Even write data
1	1H	0	X	0	0	0	1	Error	Feature
1	2H	0	X	0	0	1	0	Sector Count	Sector Count
1	3H	0	X	0	0	1	1	Sector Number	Sector Number
1	4H	0	X	0	1	0	0	Cylinder Low	Cylinder Low
1	5H	0	X	0	1	0	1	Cylinder High	Cylinder High
1	6H	0	X	0	1	1	0	Drive/Head	Drive/Head
1	7H	0	X	0	1	1	1	Status	Command
1	8H	0	X	1	0	0	0	Duplicate Even Read Data	Duplicate Even Write Data
1	9H	0	X	1	0	0	1	Duplicate Odd Read Data	Duplicate Odd Write Data
1	DH	0	X	1	1	0	1	Duplicate Error	Duplicate Feature
1	EH	0	X	1	1	1	0	Alternate Status	Device Control
1	FH	0	X	1	1	1	1	Drive Address	Reserved
1	8H	1	X	X	X	X	0	Even Read Data	Even Write Data
1	9H	1	X	X	X	X	1	Odd Read Data	Odd Write Data

9.2 Contiguous I/O Mapping Addressing

#REG	Offset	A10	A4 – A9	A3	A2	A1	A0	#IORD = "0"	#IOWR = "0"
0	0H	0	X	0	0	0	0	Even read data	Even write data
0	1H	0	X	0	0	0	1	Error	Feature
0	2H	0	X	0	0	1	0	Sector Count	Sector Count
0	3H	0	X	0	0	1	1	Sector Number	Sector Number
0	4H	0	X	0	1	0	0	Cylinder Low	Cylinder Low
0	5H	0	X	0	1	0	1	Cylinder High	Cylinder High
0	6H	0	X	0	1	1	0	Drive/Head	Drive/Head
0	7H	0	X	0	1	1	1	Status	Command
0	8H	0	X	1	0	0	0	Duplicate Even Read Data	Duplicate Even Write Data
0	9H	0	X	1	0	0	1	Duplicate Odd Read Data	Duplicate Odd Write Data
0	DH	0	X	1	1	0	1	Duplicate Error	Duplicate Feature
0	EH	0	X	1	1	1	0	Alternate Status	Device Control
0	FH	0	X	1	1	1	1	Drive Address	Reserved

9.3 Overlapping I/O Mapping Addressing

#REG	A10	A4 – A9		A3	A2	A1	A0	#IORD= "0"	#IOWR ="0"
		Primary	Secondary						
0	X	1FH	17H	0	0	0	0	Even read data	Even write data
0	X	1FH	17H	0	0	0	1	Error	Feature
0	X	1FH	17H	0	0	1	0	Sector Count	Sector Count
0	X	1FH	17H	0	0	1	1	Sector Number	Sector Number
0	X	1FH	17H	0	1	0	0	Cylinder Low	Cylinder Low
0	X	1FH	17H	0	1	0	1	Cylinder High	Cylinder High
0	X	1FH	17H	0	1	1	0	Drive/Head	Drive/Head
0	X	1FH	17H	0	1	1	1	Status	Command
0	X	3FH	37H	1	1	1	0	Alternate Status	Device Control
0	X	3FH	37H	1	1	1	1	Drive Address	Reserved

9.4 True IDE Mode

#CS0	#CS1	DA2	DA1	DA0	#IORD = "0"	#IOWR = "0"
1	1	X	X	X	Hi-Z	Not Used
1	0	0	X	X	Hi-Z	Not Used
1	0	1	0	X	Hi-Z	Not Used
0	0	X	X	X	Invalid	Invalid
1	0	1	1	0	Alternate Status	Device Control
1	0	1	1	1	Device Address	Not Used
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Feature
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	Drive/Head	Drive/Head
0	1	1	1	1	Status	Command

9.5 ATA Registers

9.5.1 Data Register

The Data Register is a 16-bit register used to transfer data blocks between the ATA data buffer and the host. In addition, the Format Track command uses this register to transfer the sector-information. Setting this mode requires calling the Set Features command.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
D7	D6	D5	D4	D3	D2	D1	D0

bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8
D15	D14	D13	D12	D11	D10	D9	D8

9.5.2 Error Register

The Error Register contains additional information about the source of an error. The information in the register is only valid when an error is indicated in ERR-bit (bit-0 = 1) of the Status Register. This register is valid when the BSY bit in Status register and Alternate status register are set to "0"(Ready).

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
BBK	UNC	MC[0]	IDNF	MCR[0]	ABRT	T0NF[0]	AMNF
BBK		Bad Block mark detected in the requested sector ID field - Not supported					
UNC		Non-Correctable data error encountered					

MC[0]	Removable media access ability has changed - not supported (is 0)
IDNF	Requested sector ID-field Not Found
MCR[0]	Media Change Request indicates that the removable-media drive's latch has changed, indicating that the user wishes to remove the media - not supported (is 0)
ABRT	Drive status error or Aborted invalid command
T0NF[0]	Track 0 Not Found during a Recalibrate command - Not supported
AMNF	Address Mark Not Found after finding the correct ID field - Not supported

9.5.3 Feature Register

This register enables drive-specific features. See the Set Features or Get/Set Features command descriptions.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Feature byte							

9.5.4 Sector Count Register

The Sector Count Register contains the number of data sectors requested to be transferred during a read or write operation between the host and the adapter. A zero register value specifies 256 sectors. The command was successful if this register is zero at command completion. If the request is not completed, the register contains the number of sectors left to be transferred.

This register's initial values is "01H". Some commands (e.g. Initialize Drive Parameters or Format Track) may redefine the register's contents.)

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Sector count byte							

9.5.5 Sector Number Register

In the CHS (Cylinder, Head, Sector) mode, the Sector Number Register contains the subsequent command's starting sector number, which can be from 1 to the maximum number of sectors per track. In LBA (logical block address) mode, this register contains LBA bits 0-7, which are updated at command completion. See the command descriptions for register contents at command completion (whether successful or unsuccessful).

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0
LBA7	LBA6	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0
SN0 – SN7		Sector number byte (8-bits)					
LBA0 – LBA7		LBA bits 0 to 7					

9.5.6 Cylinder Low Register

In the CHS mode, the Cylinder Low Register contains the cylinder number low-8 bits and reflects their status at command completion. In LBA mode, this register contains LBA bits 8-15 and reflects their status at command completion.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
LBA15	LBA14	LBA13	LBA12	LBA11	LBA10	LBA9	LBA8
CL0 – CL7		Cylinder Low byte (8-bits)					
LBA8 – LBA15		LBA bits 8 to 15					

9.5.7 Cylinder High Register

In the CHS mode, the Cylinder High Register contains the cylinder numbers high-8 bits and reflects their status at command completion. In LBA mode, this register contains LBA bits 16-23 and reflects their status at command completion.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
LBA23	LBA22	LBA21	LBA20	LBA19	LBA18	LBA17	LBA16
CH0 – CH7		Cylinder High byte (8-bits)					
LBA16 – LBA23		LBA bits 16 to 23					

9.5.8 Drive Head Register

The Drive/Head Register is used to select the drive and head (heads minus 1, when executing Initialize Drive Parameters command). It is also used to select the LBA addressing instead of the CHS addressing.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
1	LBA	1	DRV	HS3	HS2	HS1	HS0
HS0-HS3/ DRV LBA24-LBA27		Head number. Drive select number. When DRV=0, the master drive is selected. When DRV=1, the Slave drive is selected. MSB of the LBA addressing.					
LBA		Address mode select. 0 = CHS (Cylinder, Head, Sector) mode. 1 = LBA (Logical Block Address) mode. Logical Block address interrupted as follows: LBA07-LBA00 :Sector Number Register D7-D0 LBA15-LBA08:Cylinder Low Register D7-D0 LBA23-LBA16:Cylinder High Register D7-D0 LBA27-LBA24:Drive/Head Register HS3-HS0					

9.5.9 Status Register

This register contains the adapter status. The contents of this register are updated to reflect the current state of the adapter and the progress of any command being executed by the adapter. When the BSY bit is equal to zero, the other bits in this register are valid. When the BSY bit is equal to one, the other bits in this register are not valid. When the register is read, the interrupt (#IREQ pin) is cleared.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
BSY	DRDY	DWF	DSC	DRQ	CORR	0	ERR

ERR	When set, indicates that an error has occurred during the previous command execution. The bits in the Error Register indicate the cause.
IDX	Index is not used – always set to Zero.
CORR	Indicates that a data error was corrected; transfer is not terminated.
DRQ	Data Request. When set, indicates that the adapter is ready to transfer a word or byte of data between the host and the adapter.
DSC	Drive Seek Complete. When set, indicates that the requested sector was found.
DWF	Drive Write Fault status. When set, indicates that an error has occurred during write.
DRDY	Indicates whether the adapter is capable of performing drive operations (commands). This bit is cleared at power up and remains cleared until the drive is ready to accept a command. On error, DRDY changes only after the host reads the Status register.
BSY	This signal is set during the time the adapter accesses the command buffer or the registers. During this time the host is locked out from accessing the command register and buffer. As long as this bit is set no bits in the register are valid.

9.5.10 Alternate Status Register

The Alternate Status Register contains command block status information (see Status register). Unlike the Status register, reading this register does not acknowledge or clear an interrupt.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
BSY	DRDY	DWF	DSC	DRQ	CORR	0	ERR

9.5.11 Device Control Register

The Device Control Register is used to control the drive interrupt request and issue an ATA soft reset to the drive.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
---	---	---	---	1	SRST	#IEN	0

#IEN	INTERRUPT ENABLE: When set (0), it enables interrupts to the host (using the #IREQ tri-state pin). When inactive (1) or drive is not selected, it disables all pending interrupts (#IREQ in high-Z). This bit is ignored in Memory mode.
SRST	SOFT RESET: When set, forces the ATA to perform an AT disk control soft reset operation.

9.5.12 Drive Address Register

This register reflects the drive and its heads. This register is provides for compatibility with the AT disk interface. It's recommended that this register is not mapped into this host's I/O space because of potential conflicts on bit7.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
High-Z	#WTG	#HS3	#HS2	#HS1	#HS0	#DS1	#DS0
#DS0		When set (0), it indicates that drive 0 is active and selected.					
#DS1		When set (0), it indicates that drive 1 is active and selected.					
#HS0 - #HS3		Negation of the head number in the Drive/Head Register.					
#WTG		When set (0), it indicates that a write operation is in progress, otherwise it is inactive (1) - not supported.					

Note: Addressing Mode Descriptions - The adapter, on a command by command basis, can operate in either CHS or LBA addressing modes. Identify Drive Information tells the host whether the drive supports LBA mode. The host selects LBA mode via the Drive/Head Register. Sector number, Cylinder Low, Cylinder High, and Drive/Head Register bits HS3=0 contain the zero-based LBA. The drive's sectors are linearly mapped with: LBA = 0 => Cylinder 0, head 0, sector 1. Regardless of the translation mode, a sector LBA address does not change. LBA = (Cylinder * no of heads + heads) * (sectors/track) + (Sector - 1).

10. ATA Protocol Overview

Command classes are grouped according to protocols described for command execution. For all commands, the host must first check for BYS=0 before proceeding further. For most commands, the host should not proceed until DRDY=1.

10.1 PIO Data In Commands

Execution includes one more 512 bytes data-sector drive-to-host transfer. If the drive presents error status, it prepares to transfer data at the host's discretion. The host writes parameters to the Feature, Sector Count, Sector Number, Cylinder, and Drive/Head register. The host writes the Command Register's command code. The drive sets BSY and prepares for data transfer when a data sector is available; the drive sets DRQ, clears BSY, and asserts interrupt. At interrupt, the host reads the Status register, the drive negates interrupt, and the host reads one data-sector from Data Register. The drive clears DRQ. If another sector is required, the drive sets BSY and repeats the data transfer.

10.2 PIO Data Out Commands

Execution includes one or more 512 bytes host-to-drive data-sector transfers. The host writes parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head Registers. The host writes the Command register's command code. The drive sets DRQ when it can accept the first sector of data.

The host writes one sector of data to the Data register. The Drive clears DRQ and sets BSY. At sector processing complete, the drive clears BSY and asserts interrupt. If another sector transfer is required, the drive also sets DRQ. The host reads the Status register after detecting interrupt. The drive negates the interrupt if another sector transfer is required, then sequence repeats the data transfer.

10.3 Non Data Commands

Command execution involves no data transfer. The host writes parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head registers. The host writes the Command register's command code. The Drive sets BSY. When the drive completes sector processing, it clears BSY and asserts interrupt. The host reads the Status register after detecting interrupts the drive negates the interrupt.

11. Ultra DMA Data-In Commands

11.1 Initiating an Ultra DMA Data-In Burst

The following steps shall occur in the order they are listed unless otherwise specified.

a) The host shall keep DMACK- in the negated state before an Ultra DMA burst is initiated.

b) The device shall assert DMARQ to initiate an Ultra DMA burst when DMACK- is negated. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.

c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.

d) The host shall negate HDMARDY-.

e) The host shall negate CS0-, CS1-, DA2, DA1, and DA0. The host shall keep CS0-, CS1-, DA2, DA1, and DA0 negated until after negating DMACK- at the end of the burst.

f) Steps (c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts DMACK-. The host shall keep DMACK- asserted until the end of an Ultra DMA burst.

g) The host shall release DD(15:0) within t_{AZ} after asserting DMACK-.

h) The device may assert DSTROBE t_{ZIORDY} after the host has asserted DMACK-. Once the device has driven DSTROBE the device shall not release DSTROBE until after the host has negated DMACK- at the end of an Ultra DMA burst.

i) The host shall negate STOP and assert HDMARDY- within t_{ENV} after asserting DMACK-. After negating STOP and asserting HDMARDY-, the host shall not change the state of either signal until after receiving the first negation of DSTROBE from the device (i.e., after the first data word has been received).

j) The device shall drive DD(15:0) no sooner than t_{ZAD} after the host has asserted DMACK-, negated STOP, and asserted HDMARDY-.

k) The device shall drive the first word of the data transfer onto DD(15:0). This step may occur when the device first drives DD(15:0) in step (j).

l) To transfer the first word of data the device shall negate DSTROBE within t_{FS} after the host has negated STOP and asserted HDMARDY-. The device shall negate DSTROBE no sooner than t_{DVS} after driving the first word of data onto DD(15:0).

11.2 The Data-In Transfer

The following steps shall occur in the order they are listed unless otherwise specified.

a) The device shall drive a data word onto DD(15:0).

b) The device shall generate a DSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of DD(15:0). The device shall generate a DSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than t_{2cyc} for the selected Ultra DMA mode.

c) The device shall not change the state of DD(15:0) until at least t_{DVH} after generating a DSTROBE edge to latch the data.

d) The device shall repeat steps (a), (b), and (c) until the Ultra DMA burst is paused or terminated by the device or host.

11.3 Pausing an Ultra DMA Data-In Burst

The following steps shall occur in the order they are listed unless otherwise specified.

11.3.1 Device pausing an Ultra DMA Data-In Burst

a) The device shall not paused an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

b) The device shall pause an Ultra DMA burst by not generating additional DSTROBE edges. If the host is ready to terminate the Ultra DMA burst.

c) The device shall resume an Ultra DMA burst by generating a DSTROBE edge.

11.3.2 Host pausing an Ultra DMA Data-In Burst

a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

b) The host shall pause an Ultra DMA burst by negating HDMARDY-.

c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating HDMARDY-.

d) When operating in Ultra DMA modes 2, 1, or 0: If the host negates HDMARDY- within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words; or, if the host negates HDMARDY- greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. While operating in Ultra DMA modes 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words after negating HDMARDY-. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

e) The host shall resume an Ultra DMA burst by asserting HDMARDY-.

11.4 Terminating an Ultra DMA Data-In Burst

11.4.1 Device terminating an Ultra DMA Data-In Burst

Burst termination is completed when the termination protocol has been executed and DMACK- negated. The device shall terminate an Ultra DMA burst before command completion.

The following steps shall occur in the order they are listed unless otherwise specified.

a) The device shall initiate termination of an Ultra DMA burst by not generating additional DSTROBE edges.

b) The device shall negate DMARQ no sooner than t_{SS} after generating the last DSTROBE edge. The device shall not assert DMARQ again until after DMACK- has been negated.

c) The device shall release DD(15:0) no later than t_{AZ} after negating DMARQ.

d) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall

not negate STOP again until after the Ultra DMA burst is terminated.

e) The host shall negate HDMARDY- within t_{LI} after the device has negated DMARQ. The host shall continue to negate HDMARDY- until the Ultra DMA burst is terminated. Steps (d) and (e) may occur at the same time.

f) The host shall drive DD(15:0) no sooner than t_{ZAH} after the device has negated DMARQ. For this step, the host may first drive DD(15:0) with the result of the host CRC calculation.

g) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.

h) If the host has not placed the result of the host CRC calculation on DD(15:0) since first driving DD(15:0) during (f), the host shall place the result of the host CRC calculation on DD(15:0).

i) The host shall negate DMACK- no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY-, and no sooner than t_{DVS} after the host places the result of the host CRC calculation on DD(15:0).

j) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.

k) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command the device shall report the first error that occurred.

l) The device shall release DSTROBE within t_{IORDYZ} after the host negates DMACK-.

m) The host shall not negate STOP nor assert HDMARDY- until at least t_{ACK} after negating DMACK-.

n) The host shall not assert DIOR-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

11.4.2 Host terminating an Ultra DMA Data-In Burst

The following steps shall occur in the order they are listed unless otherwise specified.

a) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.

b) The host shall initiate Ultra DMA burst termination by negating HDMARDY-. The host shall continue to negate HDMARDY- until the Ultra DMA burst is terminated.

c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating HDMARDY-.

d) When operating in Ultra DMA modes 2, 1, or 0: If the host negates HDMARDY- within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words; or, if the host negates HDMARDY- greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. While operating in Ultra DMA modes 4 or

3 the host shall be prepared to receive zero, one, two or three additional data words after negating HDMARDY-. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

e) The host shall assert STOP no sooner than t_{RP} after negating HDMARDY-. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

f) The device shall negate DMARQ within t_{LI} after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

g) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.

h) The device shall release DD(15:0) no later than t_{AZ} after negating DMARQ.

i) The host shall drive DD(15:0) no sooner than t_{ZAH} after the device has negated DMARQ. For this step, the host may first drive DD(15:0) with the result of the host CRC calculation .

j) If the host has not placed the result of the host CRC calculation on DD(15:0) since first driving DD(15:0) during (9), the host shall place the result of the host CRC calculation on DD(15:0).

k) The host shall negate DMACK- no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY-, and no sooner than t_{DVS} after the host places the result of the host CRC calculation on DD(15:0).

l) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.

m) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred.

n) The device shall release DSTROBE within t_{IORDYZ} after the host negates DMACK-.

o) The host shall neither negate STOP nor assert HDMARDY- until at least t_{ACK} after the host has negated DMACK-.

p) The host shall not assert DIOR-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

11.5 Ultra DMA Data-Out Commands

11.5.1 Initiating an Ultra DMA Data-Out Burst

The following steps shall occur in the order they are listed unless otherwise specified.

a) The host shall keep DMACK- in the negated state before an Ultra DMA burst is initiated.

b) The device shall assert DMARQ to initiate an Ultra DMA burst when DMACK- is negated.

c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.

d) The host shall assert HSTROBE.

e) The host shall negate CS0-, CS1-, DA2, DA1, and DA0. The host shall keep CS0-, CS1-, DA2, DA1, and DA0 negated until after negating DMACK- at the end of the burst.

f) Steps (c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts DMACK-. The host shall keep DMACK- asserted until the end of an Ultra DMA burst.

g) The device may negate DDMARDY- t_{ZIORDY} after the host has asserted DMACK-. Once the device has negated DDMARDY-, the device shall not release DDMARDY- until after the host has negated DMACK- at the end of an Ultra DMA burst.

h) The host shall negate STOP within t_{ENV} after asserting DMACK-. The host shall not assert STOP until after the first negation of HSTROBE.

i) The device shall assert DDMARDY- within t_{LI} after the host has negated STOP. After asserting DMARQ and DDMARDY- the device shall not negate either signal until after the first negation of HSTROBE by the host.

j) The host shall drive the first word of the data transfer onto DD(15:0). This step may occur any time during Ultra DMA burst initiation.

k) To transfer the first word of data: the host shall negate HSTROBE no sooner than t_{UI} after the device has asserted DDMARDY-. The host shall negate HSTROBE no sooner than t_{DVS} after the driving the first word of data onto DD(15:0).

11.5.2 The Data-Out Transfer

The following steps shall occur in the order they are listed unless otherwise specified.

a) The host shall drive a data word onto DD(15:0).

b) The host shall generate an HSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of DD(15:0). The host shall generate an HSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than t_{2cyc} for the selected Ultra DMA mode.

c) The host shall not change the state of DD(15:0) until at least t_{DVH} after generating an HSTROBE edge to latch the data.

d) The host shall repeat steps (a), (b), and (c) until the Ultra DMA burst is paused or terminated by the device or host.

11.5.3 Pausing an Ultra DMA Data-Out Burst

The following steps shall occur in the order they are listed unless otherwise specified.

11.5.4 Host pausing an Ultra DMA Data-Out Burst

a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

b) The host shall pause an Ultra DMA burst by not generating an HSTROBE edge. If the host is ready to terminate the Ultra DMA burst.

c) The host shall resume an Ultra DMA burst by generating an HSTROBE edge.

11.5.5 Device pausing an Ultra DMA Data-Out Burst

a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

b) The device shall pause an Ultra DMA burst by negating DDMARDY-.

c) The host shall stop generating HSTROBE edges within t_{RFS} of the device negating DDMARDY-.

d) When operating in Ultra DMA modes 2, 1, or 0: If the device negates DDMARDY- within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words; or, if the device negates DDMARDY- greater than t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. While operating in Ultra DMA modes 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words after negating DDMARDY-. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.

e) The device shall resume an Ultra DMA burst by asserting DDMARDY-.

11.5.6 Terminating an Ultra DMA Data-Out Burst

The following steps shall occur in the order they are listed unless otherwise specified.

11.5.7 Host terminating an Ultra DMA Data-Out Burst

a) The host shall initiate termination of an Ultra DMA burst by not generating additional HSTROBE edges.

b) The host shall assert STOP no sooner than t_{SS} after the last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

c) The device shall negate DMARQ within t_{LI} after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

d) The device shall negate DDMARDY- within t_{LI} after the host has negated STOP. The device shall not assert DDMARDY- again until after the Ultra DMA burst termination is complete.

e) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.

f) The host shall place the result of the host CRC calculation on DD(15:0)

g) The host shall negate DMACK- no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY-, and no sooner than t_{DVS} after placing the result of the host CRC calculation on DD(15:0).

h) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.

i) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA

bursts for any one command, at the end of the command, the device shall report the first error that occurred.

j) The device shall release DDMARDY- within t_{IORDYZ} after the host has negated DMACK-.

k) The host shall neither negate STOP nor negate HSTROBE until at least t_{ACK} after negating DMACK-.

l) The host shall not assert DIOW-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

11.5.8 Device terminating an Ultra DMA Data-Out Burst

Burst termination is completed when the termination protocol has been executed and DMACK- negated. The device shall terminate an Ultra DMA burst before command completion. The following steps shall occur in the order they are listed unless otherwise specified.

a) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.

b) The device shall initiate Ultra DMA burst termination by negating DDMARDY-.

c) The host shall stop generating an HSTROBE edges within t_{RFS} of the device negating DDMARDY-.

d) When operating in Ultra DMA modes 2, 1, or 0: If the device negates DDMARDY- within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words; or, if the device negates DDMARDY- greater than t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. While operating in Ultra DMA modes 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words after negating DDMARDY-. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.

e) The device shall negate DMARQ no sooner than t_{RP} after negating DDMARDY-. The device shall not assert DMARQ again until after DMACK- is negated.

f) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

g) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.

h) The host shall place the result of the host CRC calculation on DD(15:0).

i) The host shall negate DMACK- no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY-, and no sooner than t DVS after placing the result of the host CRC calculation on DD(15:0).

j) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.

k) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA

bursts for any one command, at the end of the command, the device shall report the first error that occurred.

l) The device shall release DDMARDY- within t_{IORDYZ} after the host has negated DMACK-.

m) The host shall neither negate STOP nor HSTROBE until at least t_{ACK} after negating DMACK-.

n) The host shall not assert DIOW-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

11.6 Ultra DMA CRC Rules

The following is a list of rules for calculating CRC, determining if a CRC error has occurred during an Ultra DMA burst, and reporting any error that occurs at the end of a command.

a) Both the host and the device shall have a 16-bit CRC calculation function.

b) Both the host and the device shall calculate a CRC value for each Ultra DMA burst.

c) The CRC function in the host and the device shall be initialized with a seed of 4ABAh at the beginning of an Ultra DMA burst before any data is transferred.

d) For each STROBE transition used for data transfer, both the host and the device shall calculate a new CRC value by applying the CRC polynomial to the current value of their individual CRC functions and the word being transferred. CRC is not calculated for the return of STROBE to the asserted state after the Ultra DMA burst termination request has been acknowledged.

e) At the end of any Ultra DMA burst the host shall send the results of the host CRC calculation function to the device on DD(15:0) with the negation of DMACK-.

f) The device shall then compare the CRC data from the host with the calculated value in its own CRC calculation function. If the two values do not match, the device shall save the error. A subsequent Ultra DMA burst for the same command that does not have a CRC error shall not clear an error saved from a previous Ultra DMA burst in the same command. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.

g) For READ DMA, WRITE DMA, READ DMA QUEUED, or WRITE DMA QUEUED commands: When a CRC error is detected, the error shall be reported by setting both ICRC and ABRT (bit 7 and bit 2 in the Error register) to one. ICRC is defined as the “Interface CRC Error” bit. The host shall respond to this error by re-issuing the command.

h) For a REQUEST SENSE packet command (see SPC T10/955D for definition of the REQUEST SENSE command): When a CRC error is detected during transmission of sense data the device shall complete the command and set CHK to one. The device shall report a Sense key of 0Bh (ABORTED COMMAND). The device shall preserve the original sense data that was being returned when the CRC error occurred. The device shall not report any additional sense data specific to the CRC error. The host device driver may retry the REQUEST SENSE command or may consider this an unrecoverable error and retry the command that caused the Check Condition.

i) For any packet command except a REQUEST SENSE command: If a CRC error is

detected, the device shall complete the command with CHK set to one. The device shall report a Sense key of 04h (HARDWARE ERROR). The sense data supplied via a subsequent REQUEST SENSE command shall report an ASC/ASCQ value of 08h/03h (LOGICAL UNIT COMMUNICATION CRC ERROR). Host drivers should retry the command that resulted in a HARDWARE ERROR.

j) A host may send extra data words on the last Ultra DMA burst of a data-out command. If a device determines that all data has been transferred for a command, the device shall terminate the burst. A device may have already received more data words than were required for the command. These extra words are used by both the host and the device to calculate the CRC, but, on an Ultra DMA data-out burst, the extra words shall be discarded by the device.

k) The CRC generator polynomial is: G(X) = X16 + X12 + X5 + 1. Table 46 describes the equations for 16- bit parallel generation of the resulting polynomial (based on a word boundary).

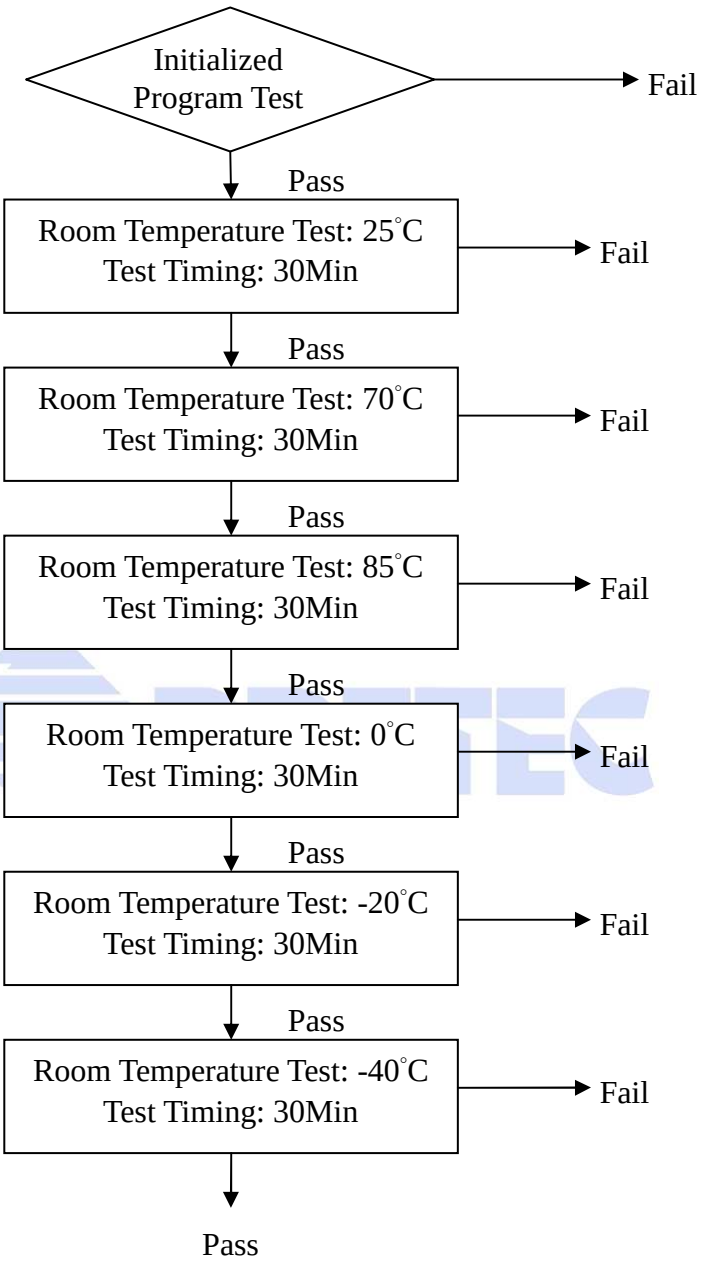
NOTE:

Since no bit clock is available, the recommended approach for calculating CRC is to use a word clock derived from the bus strobe. The combinational logic is then equivalent to shifting sixteen bits serially through the generator polynomial where DD0 is shifted in first and DD15 is shifted in last.

If excessive CRC errors are encountered while operating in an Ultra mode, the host should select a slower Ultra mode. Caution: CRC errors are detected and reported only while operating in an Ultra mode.

12. System Environmental Specifications

12.1 Temperature Test Flow



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